# 5.2-GHz Direct-Conversion CMOS Receiver

ECE215C Analysis and Design of RF Circuits and System – Final Project Report

Runzhou Chen
Department of Electrical and Computer Engineering
University of California, Los Angeles
Los Angeles, USA
runzhouchen@gmail.com

Jiayu Wang
Department of Electrical and Computer Engineering
University of California, Los Angeles
Los Angeles, USA
jywang0205@g.ucla.edu

***Abstract*—This is the final project of ECE215C (Analysis and Design of RF Circuits and System) about designing a 5.2GHz direct-conversion CMOS receiver with requirements of Noise Figure, $IIP_3$, Input Resistance, Output Resistance, Phase noise, and Receiver Gain. This report clearly states how each block, including Low Noise Amplifier (LNA), Mixer, Local Oscillator (LO), and Divide-by-2 Circuits, is designed step by step from the topology structure variable choice and also includes the simulation result with the plot.**

***Keywords—Direct-Conversion Receiver, Noise Figure, LNA, Mixer, LO, RF.***

## I. Introduction

This report describes the design steps, variable analysis, and simulation results of a 5.2GHz direct-conversion CMOS receiver consists four main blocks, including LNA, Mixer, LO, and Divide-by-2 circuits (we have one more stage so totally of 5 blocks), as shown in figure 1. The final receiver achieves a 3.5dB noise figure, -10dBm $IIP_3$, and 30dB receiver gain with 50Ω input resistance and 1000Ω output resistance.

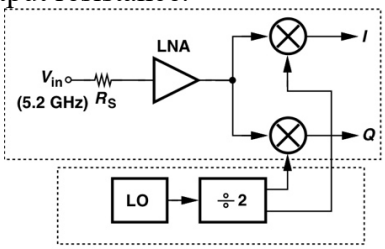


Fig. 1. Circuit Block Diagram of the Receiver

## II. Low Noise Amplifier Design

### A. Design Idea Procedure

For the LNA design, we used common-source (CS) cascode topology with inductive degeneration and folded PMOS IMD sinker. The CS stage is chosen since the noise figure is better than the common-gate (CG), and we use cascode for better reverse isolation and gain boosting. The inductive degeneration provides higher linearity and output resistance. However, the drawback of CS cascode stems from its bad $IIP_3$ and we applied a folded PMOS IMD sinker based on the work in [1] to enhance its linearity. Meanwhile, we introduced a capacitor between the gate and source of the input stage to decouple the input resonant circuit Q and Cgs, improving the noise figure. The circuit schematic is shown in figure 2.

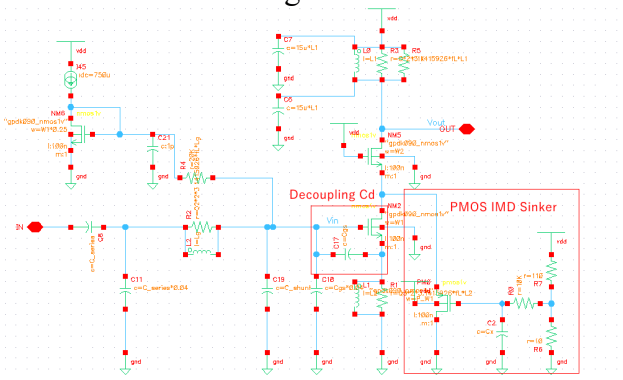


Fig. 2. LNA Circuit Schematic in Cadence

### B. Design Variable Analysis

The DC biasing was chosen for the optimal MOSFET performance. For a single CS stage with width $W_1$ = 30u, we plotted gm, NF, and gain with respect to the gate voltage, as shown in figure 3. We wish to achieve the maximum possible gm while avoiding velocity saturation. From the waveform, we observed an optimal biasing point for width $W_1$ = 30um with gate voltage = 500mV.

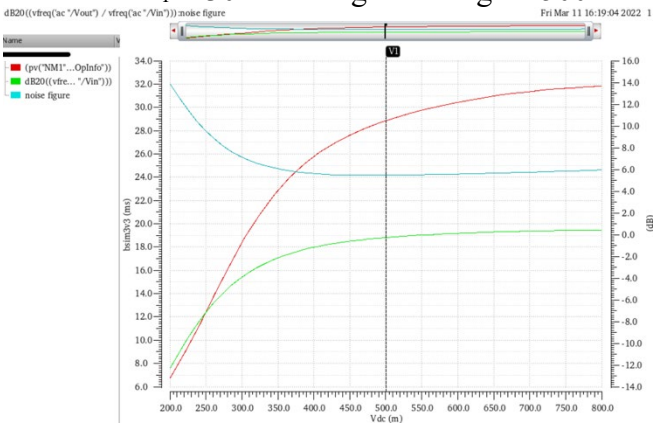


Fig. 3. Gm, NF, and Gain vs. $V_{Gate}$

The second issue is impedance matching. According to the calculation, the input impedance of the CS stage with inductive degeneration is given by $Zin = \frac{gm*Ls}{Cgs} + j[\omega(Ls + Lg) - \frac{1}{\omega 0*Cgs}]$, as the source resistance Rs = 50 ohms, we need to

have $gm \times \frac{Ls}{Cgs} = 50$ and $w0 \times (Ls + Lg) = \frac{1}{w0} \times Cgs$. Using the DC analysis, we found that the Cgs under given bias voltage is 35 fF. Then we started with Ls = 1nH and performed the S-parameter simulation with the Smith chart, and obtained the best matching network.

To improve the noise figure of LNA, we took the approach mentioned in [2]. The basic idea is to introduce another capacitor Cd in parallel with the Cgs of the MOSFET. This capacitor can decouple the input Q from Cgs, which allows for an adjustable reduction of Q for any value of Cgs; hence the gate current noise is also reduced. By doing simulations, we verified that the NF decreased by 0.5dB.

The most significant issue is to improve the linearity since that of the CS stage is usually troublesome. The work from [1] introduced an intermodulation distortion (IMD) sinker between the cascode stages for better linearity. The basic idea is that an additional folded cascode PMOS absorbs the 3rd harmonic intermodulation current generated by the CS FET. The IMD sinker will lead to a slightly lower gain and higher NF, but the degradation is not severe. According to the simulations, the $IIP_3$ of the LNA raised from -13dBm to -1dBm but the IMD sinker.

We finalized our LNA design with the variable shown in Table I.

TABLE I. VARIABLES OF LNA DESIGN

| $L_1$ | $L_g$ | $L_s$ | $C_{Series}$ | $C_{Shunt}$ | $W_1$ | $W_2$ | $C_{GS}$ |
|---|---|---|---|---|---|---|---|
| 5.9nH (Q = 8) | 10 n (Q = 30) | 1.1nH (Q = 15) | 150fF | 115fF | 25u | 35u | 71fF |

## C. Simulation Result

### 1) Input Resistance

From the Smith Chart shown in figure 4, we achieved that the input resistance = 50Ω and the input reactance = 0Ω

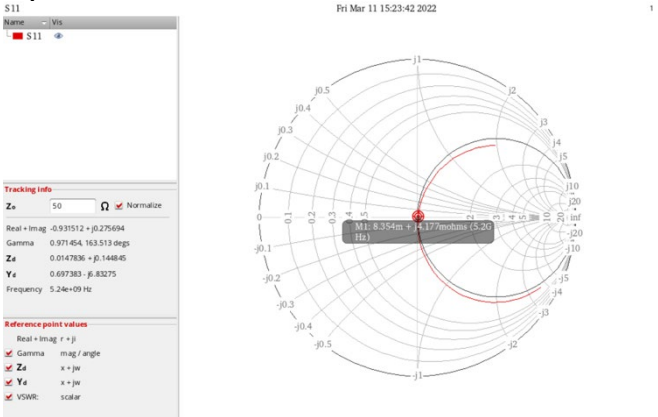


Fig. 4. Smith Chart for Input Resistance and Reactance

### 2) $IIP_3$ & Gain

We apply a two-tone test with a voltage amplitude of 10mV at 5.2GHz and 5.21GHz. From the figure 5, we can find that:

- $IIP_3$ = -30dBm + (-30 dB+ 88dB) / 2 = -1dBm (Satisfy our expectation)
- Gain = 10dB (not outstanding but acceptable due to better $IIP_3$ performance. We will introduce a new block of differential pair to improve the gain, which will be reported in Part VI.)

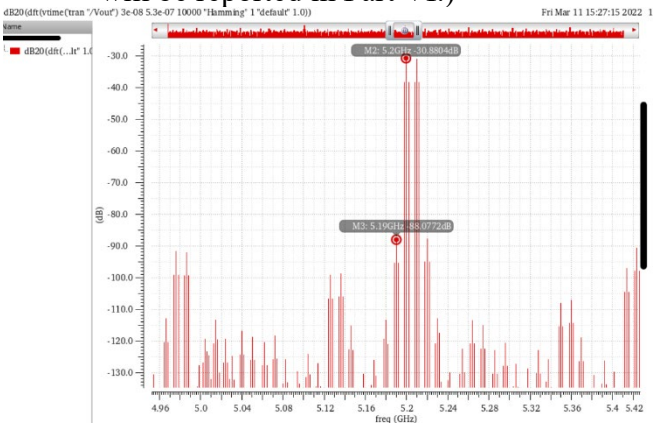


Fig. 5. $IIP_3$ and Gain Value in tran Simulation

### 3) Noise Figure

We performed a pss and pnoise simulation for the noise figure. From figure 6, we can find that the NF of our designed LNA is 2.75dB, which satisfies our expectation.

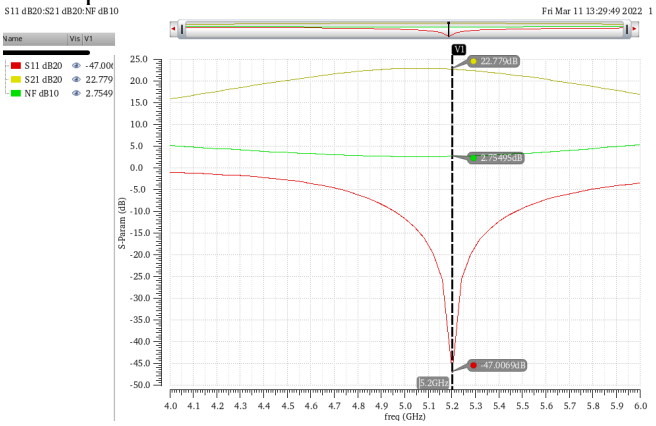


Fig. 6. Noise Figure Value in pss and pnoise Simulation

# III. MIXER DESIGN

## A. Design Procedure

For the mixer design, we decided to use the active single sideband mixer topologies and the circuit schematic in figure 7 shown [3]. In this structure, there are six variables – $R_{Load}$, $C_{Load}$, $W_1$, $W_{2,3}$, and $V_{Bias}$, which we need to adjust to reach the expected $IIP_3$, conversion gain, and NF.

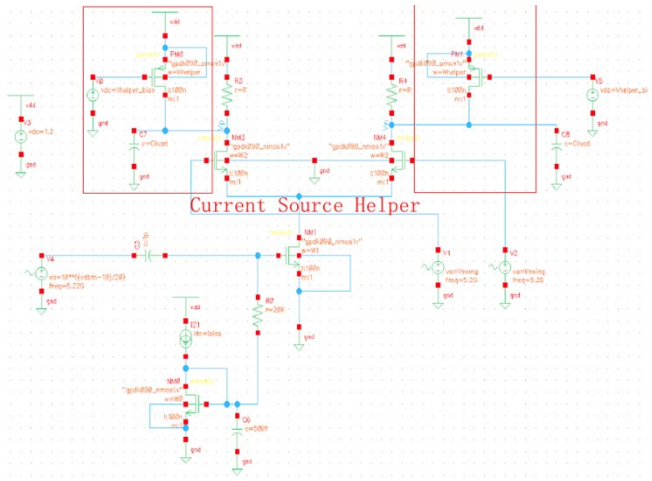


Fig. 7. Active Mixer Circuit Schematic in Cadence

### B. *Requirement Analysis and Expectation*

For these four requirements:

- Conversion gain $= \frac{2}{\pi} gm_1 * R_{load}$
- $IIP_3 \propto V_{GS} - V_{TH}$
- $NF = 1 + \frac{\pi^2 kT\left(\frac{\gamma}{gm1} + \frac{2}{gm1^2 Rload}\right)}{4kTR_S}$
- Make all transistors work in the saturation region: $V_{DS} > V_{GS} - V_{TH}$

For our first expectation, we expected a mixer with:

- 5dB gain
- 5 ~ 8dB noise figure
- A-10dBm $IIP_3$ where A represents the gain of LNA from Friis Equation.
- Friis Equation: $\frac{1}{AIP3^2} \approx \frac{1}{A^2 IP3,1} + \frac{\alpha 1^2}{A^2 IP3,2}$

### C. *Design Variable Analysis*

First, we began with DC simulation with an approximately bias voltage of 600mV. To have a good mixer performance, the circuit needs to have a relatively high W/L ratio, high bias current, and high load resistance. Then we distributed the 1.2V to each stage and tried to make them be like: load resistor - 600mV, LO stage - 300mV, and RF stage - 300mV. Then the W/L ratio was adjusted so that for the LO stage, $V_{GS}$ is very close to $V_{TH}$ since when the AC LO voltage is slightly higher than 0V, the MOSFET is turned on and vice versa. Meanwhile, the W/L of the RF stage was adjusted so that the gm is high for the voltage conversion gain and the overdrive voltage is not too high to maintain the linearity. Lastly, we chose the load resistor based on the equation of gain, which increased from 100 ohms to enlarge the gain, whereas a too-large resistor may result in a bad NF, so we chose $R_{Load} = 450\ \Omega$.

During the design process, we added an innovation point – current helper because of the poor performance of gain (the load resistor is too high to allow large current and hence a low gain) and $IIP_3$ (input transistor current is too low to meet the requirement). Even if it increases the noise figure, we still want it to our design due to the flexibility of NF in our mixer. Figure 7 already shows the version with the current helper.

Finally, after several attempts on those variables and requirements, we finalized our value, as shown in Table II.

TABLE II. VARIABLES OF ACTIVE MIXER DESIGN

| $I_{Bias}$ | $R_{Load}$ | $C_{Load}$ | $Helper_{Bias}$ | $W_0$ | $W_1$ | $W_{2,3}$ | $W_{Helper}$ | LO-DC | LO-AC |
|---|---|---|---|---|---|---|---|---|---|
| 300uA | 450Ω | 10pF | 550mV | 10um | 35um | 25um | 6um | 600mV | 600mV |

### D. *Simulation Result*

#### 1) *DC Simulation*

We performed DC analysis, and checked the operating points of each device. We made sure that each MOSFET was working in saturation.

#### 2) *Gain & $IIP_3$*

To test the approximate voltage conversion gain, we use 10mV amplitude with two tones (5.22GHz and 5.23GHz) to do both Gain and $IIP_3$ testing. Since the LO we set provides a 5.2GHz signal, the ideal two tones of the output should be 20MHz and 30MHz, and thus we looked at the difference between 10MHz and 20MHz for $IIP_3$ calculation. We used transient simulation with 1us and send the waveform to DFT and dB20 to see the gain. In the below figure 8, we find the following value:

- Gain = -32.958dB – (-40dB) ≅ 7dB (Satisfies our expectation)
- $IIP_3$ = (-32.958 – (-83.064))/2 – 30dB = -4.95dBm (Satisfies our expectation)

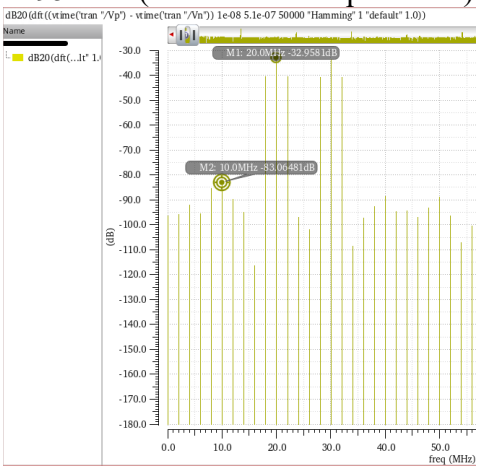


Fig. 8. $IIP_3$ and Gain Value in tran Simulation

*3) Noise Figure*

We performed a pss and pnoise simulation for the NF. From figure 9, we found that the NF of our designed mixer is 6.48dB, which satisfies our expectations.

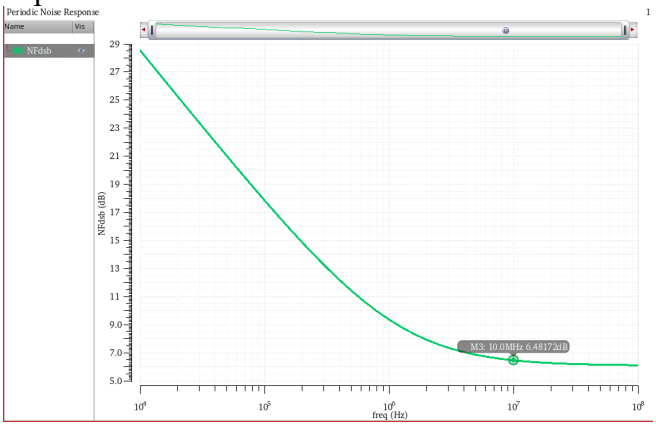


Fig. 9. Noise Figure Value in pss and pnoise Simulation

## IV. Local Oscillator Design

### A. Design Idea Procedure

We design the oscillator based on the concept of impulse sensitivity function (ISF) in Hajimiri's phase noise model [4]. The impulse sensitivity function (ISF) describes the oscillator output phase noise sensitivity to the injected noises into the tank circuit in terms of time. A typical cross-coupled oscillator has a significant phase noise since the tail current is large during the time that ISF is at maximum, which is the zero-crossing time of the waveform. To reduce the waveform, the work in [5] raised the point that if the tail current can be reduced during the zero-crossing time (i.e., ISF is large), the phase noise can be reduced.

The above tail-current shaping method mentioned in [5] can reduce the phase noise to a large extent. To do this, we applied a cascode structure based on the classic cross-coupled oscillator. The basic idea is that, during the waveform zero-crossing, the lower two MOSFETs are biased slightly above the threshold and thus provide a large overdrive voltage. The Vds of the current source are reduced, and so is the tail current. On the other hand, when one output waveform reaches the peak, one of the lower MOSFETs will be fully turned on, and the Vds of the current source is increased, together with the tail current. The finalized LO circuit schematic is shown in figure 10.

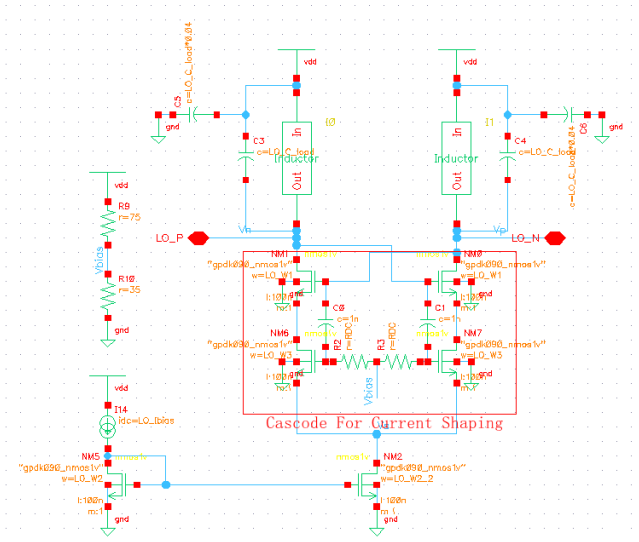


Fig. 10. LO Circuits Schematic in Cadence.

### B. Simulation Result & Variable Analysis

We performed a simulation to compare the waveform and phase noise of the oscillator with and without the cascode structure. From the phase noise comparison shown in figure 11, we see that the cascode structure can improve the oscillator's phase noise by 10dBc/Hz at the offset frequency of 1MHz.

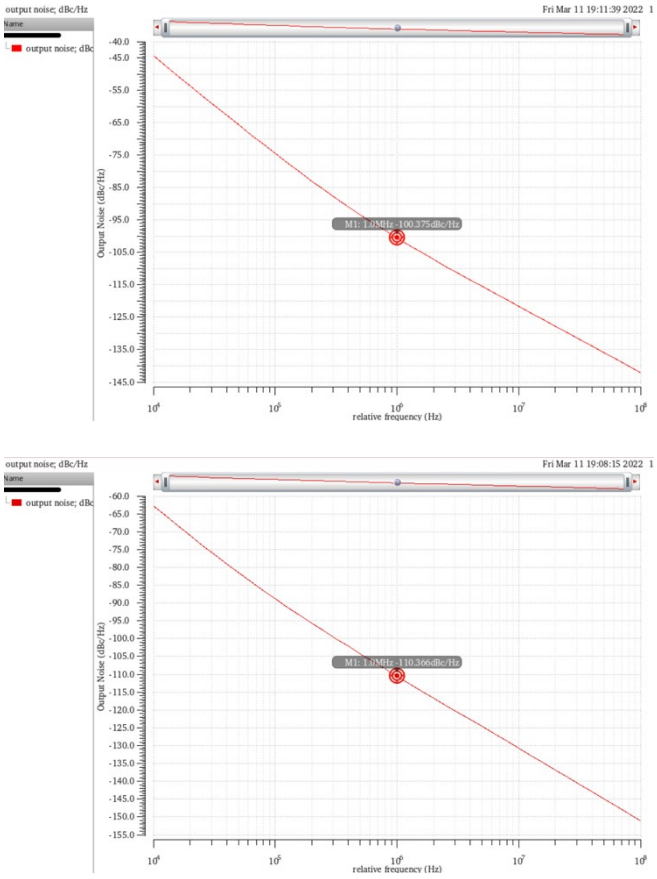


Fig. 11. Phase Noise Comparison for cascode circuit and without cascode circuit.

The waveform of voltage (left) and current (right) can explain the function of tail-current shaping. The red curves in the left and right plots in figure 12 represent the current source Vds and Id, respectively. We can observe that, at a zero-crossing time (e.g., 2ns), the Vds of the current source is reduced to 35mV, in comparison to its maximum value, which is 154mV. Similarly, the tail current is reduced from 8.4mA to 2mA at 2ns. The tail-current shaping can guarantee that minimum tail current is delivered when ISF is maximum. The phase noise is therefore reduced.

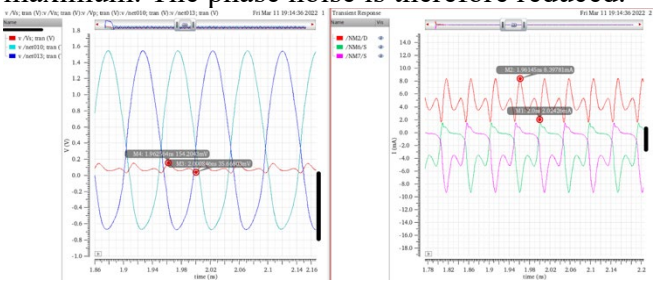

Fig. 12. The waveform of Voltage (Left) and Current (right)

The finalized variable values of the LO circuit are shown in Table III.

TABLE III. VARIABLES OF LO CIRCUIT DESIGN

| $V_{Bias}$ | $I_{Bias}$ | Q | $R_P$ | $W_1$ | $W_2$ |
|---|---|---|---|---|---|
| 350mV | 4mA | 8 | 800Ω | 30um | 10um |
| **$W_3$** | **$W_{2-2}$** | **$C_{Load}$** | **Frequency** | **$L_1$** | **$R_{DC}$** |
| 20um | 40um | 13fF | 10.4GHz | 865pH | 5kΩ |

## V. DIVIDE-BY-TWO CIRCUIT DESIGN

### A. *Design Procedure and Variables Choocing*

We applied the cascode switch logic to achieve each latch for this circuit implementation. The below figure 13 shows the circuit schematic of a latch. In each latch circuit, there are three variables, the width of M1, M3, and M5. The standard for choosing their values is to ensure that the M1 in series with M5 must overcome M3. From the textbook, in the typical design, $W_5 \approx W_{1,2} \approx 2 \times W_{3,4}$ and speed requirements may encourage a wider W5. But in this case, we need to drive a signal with 10.4GHz, so we assumed a higher $W_5$ to make the divider work. Finally, we chose the value shown in Table IV to make sure that when the input signal is 10.4GHz, the output is a square wave with 5.2GHz (later we combine it with LO and let it generate a signal with 5.19GHz as the LO input of the mixer by changing the LO side). In single block testing, we use 10.4GHz as a test source.

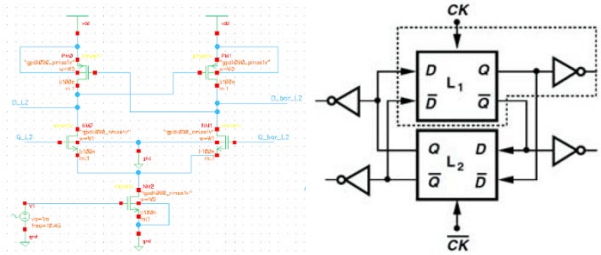


Fig. 13. Latch Circuit Schematic and Diagram of Two Latches Combination

The below figure 14 shows the complete schematic design of our divide-by-2 circuit. When we finished the design of each latch, we combine them like the below figure shows. For the inverter, we chose $W_P$ = 6um and $W_N$ = 3um to make it work as a buffer.

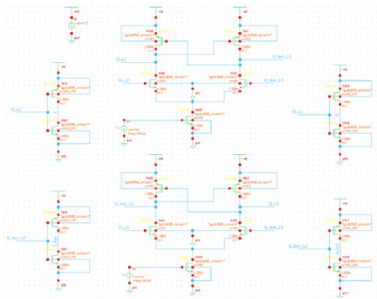

Fig. 14. Divide-by-2 Circuit Schematic in Cadence

TABLE IV. VARIABLES OF DIVIDE-BY-2 CIRCUIT DESIGN

| $W_1$ | $W_3$ | $W_5$ | $W_P$ | $W_N$ |
|---|---|---|---|---|
| 7um | 7um | 40um | 6um | 3um |

### B. *Simulation Result*

We used a sinusoid input waveform with 10.4GHz to test. The below figure 15 show the square waveform of output I & I_Bar and output Q & Q_Bar, which is our expectation.

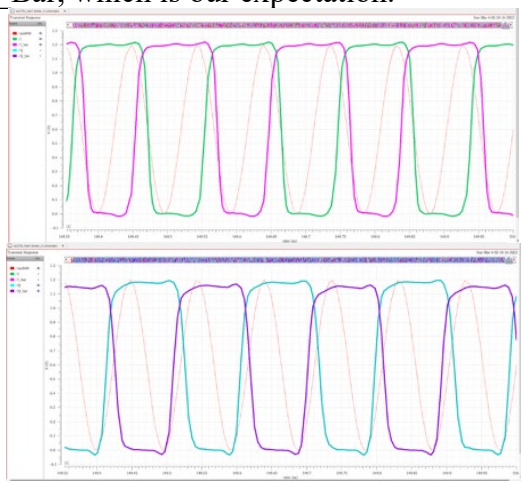

Fig. 15. Simulation Output of I & I_bar and Q & Q_bar

Also, for the frequency check, we did a calculation. From the below figure 16, we find the

- Period = 149.55 - 149.36 = 0.19ns
- Frequency = 1/ 0.192ns = 5.208GHz

The divide-by-2 circuit satisfied the requirement.

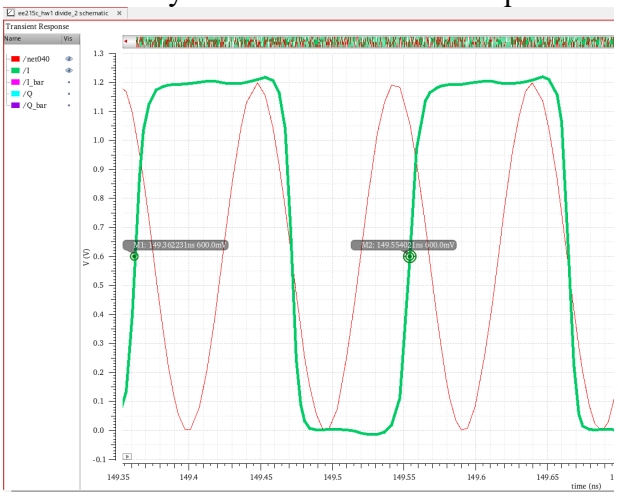

Fig. 16. Frequency Calculation Point of Output I

## VI. Additional Stage – Differential Pair

When we finished the original four parts of the receiver and combine them, we found a tradeoff between the whole receiver's gain and $IIP_3$. Because the $IIP_3$ was hard to adjust, we chose to sacrifice the gain of LNA to get better $IIP_3$ performance. Due to the time limitation and circuit complexity, we decided to use simple differential pair as an additional stage to improve the overall receiver gain.

### A. Design Procedure

Shown in figure 17, we have the basic circuit schematic. We had six variables - $C_{Load}$, $R_{Load}$, $I_{Bias}$, $W_0$, $W_1$, $W_{2,3}$ to decide our circuit performance. We combined the differential pair with our mixer to see the overall performance.

### B. Requirement Analysis and Expectations

In the differential pair, theoretically, the gain equals to $gm_1 \times R_{load}$ while keeping all-transistor working in the saturation region. We hope to let the additional stage provide 10dB more gain (totally about 18dB for mixer and differential pair) while keeping the $IIP_3$ not changing too much.

### C. Design Variable Analysis

According to the equation $Gain = gm_1 \times RLoad = 10dB = 3$, we first perform a bias current of 500uA to see its performance. The W/L ratio is adjusted so that $V_{GS}$ is very close to $V_{TH}$ for differential pairs to turn the MOSFET on. Meanwhile, the W/L was adjusted so that the gm is high for the voltage conversion gain and the overdrive voltage is not too high to maintain the linearity. Lastly, we choose the load resistor based on the equation of gain, which increased from 100 ohms to enlarge the gain, whereas a too-large resistor may result in a bad NF, so we chose $R_{Load}$ = 550 Ω.

Finally, after several attempts on those variables and requirements, we finalized our value, as Table V shows.

TABLE V. VARIABLES OF DIFFERENTIAL PAIR CIRCUIT DESIGN

| $I_{Bias}$ | $R_{Load}$ | $C_{Load}$ | $W_0$ | $W_1$ | $W_{2,3}$ |
|---|---|---|---|---|---|
| 800uA | 550Ω | 10pF | 5um | 5um | 35um |

### D. Simulation Result

In this simulation part, we connect the mixer with the differential pair stage to see the overall performance of DC, Gain, $IIP_3$, and NF.

#### 1) DC Simulation

We performed DC analysis, and the operating points of each device are shown in figure xx. We make sure that each MOSFET is working in saturation mode.

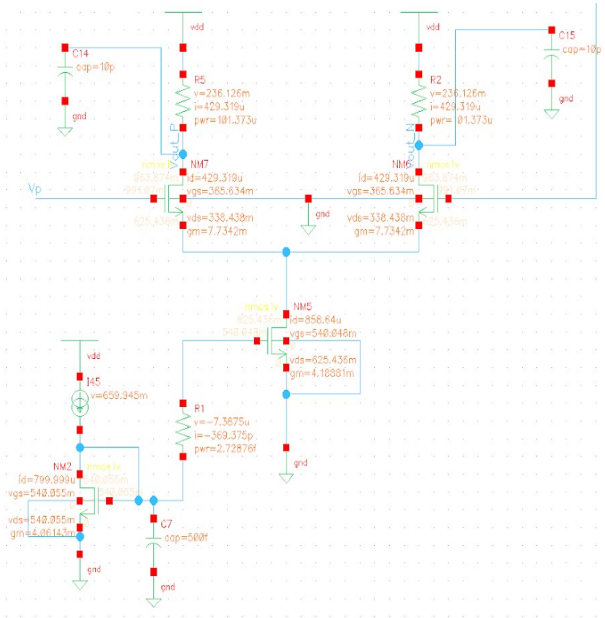

Fig. 17. Operating Point of Differential Pair in DC Analysis

#### 2) Gain & $IIP_3$

We used the same setting as we test the mixer. In the below figure 18, we find the following value:

- Gain = -20.827dB – (-40dB) ≅ 19dB (Satisfy our expectation)
- $IIP_3$ = (-22.827 – (-72.678))/2 – 30dB = -5.07dBm

(Satisfy our expectation without too much change compared with only mixer)

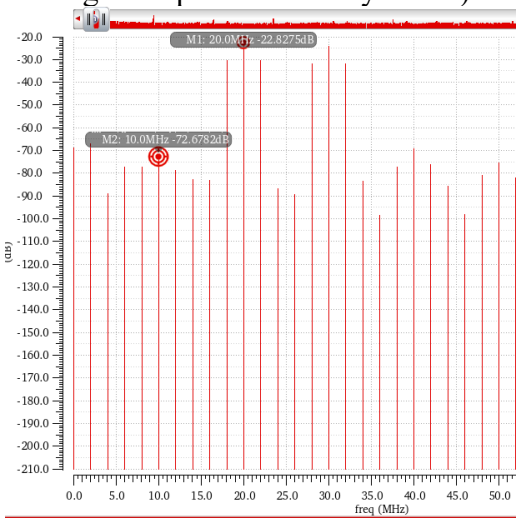


Fig. 18. $IIP_3$ and Gain Value in tran Simulation

*3) Noise Figure*

We performed a pss and pnoise simulation for the noise figure. From figure 19, we can find that the NF of our designed mixer is 5.78dB, which satisfies our expectations.

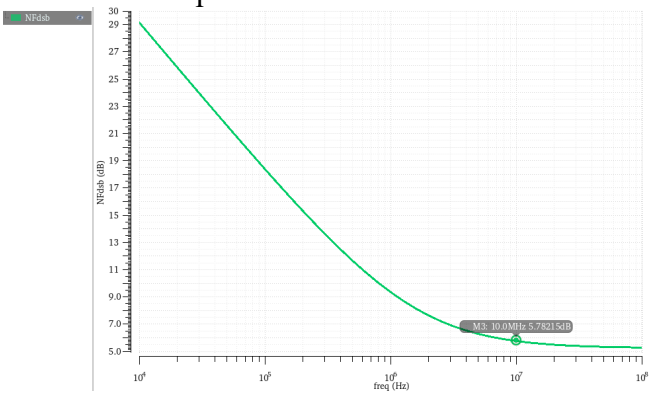


Fig. 19. Noise Figure Value in pss and pnoise Simulation

## VII. Circuit Combination and Simulation

After we finished the design of each block, we combined the circuits with seeing the performance of the overall circuits. First, we combined the LNA, Mixer, and Differential pair as the upper block and combine the LO with the Divide-by-2 circuit as the lower block.

We wanted to check the upper block's gain, $IIP_3$, and noise figure. We wanted to check the Phase noise for the lower block and whether the output frequency equals 5.19GHz.

### *A. Upper Block Simulation*

Figure 20 shows the upper block circuits combination and do the simulation. We doubled the mixer for the I and Q mixer and combine them into a differential pair for amplification.

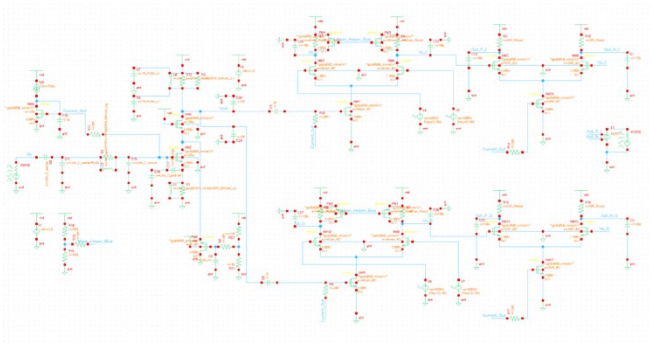

Fig. 20. Upper Block Circuit Schematic in Cadence

During the simulation process, we changed variables like the width of the switching transistor and bias current. When the simulation result did not meet our expectations, we checked the circuit block by block to see which block had the unexpected value and did the change correspondingly. Also, since we can only have one ideal current source per block, we change the ideal current source by implementing a voltage divider and current mirror. The finalized parameters are shown in Table VI in the conclusion part. Figures 21 to 24 show the simulation result of noise figure, $IIP_3$, and Gain.

- Noise Figure @ 10MHz: 3.41dB
- $IIP_3$ = -30dBm+(-15dB+55dB)/2 = -10dBm by applying two-tone :10mV with 5.21GHz, 5.22GHz with LO = 5.19GHz
- Voltage Conversion Gain = 20log (182.4m/(0.5*10m)) = 31.2dB from 5.2GHz to 10MHz
- Output Resistance = 229Ω

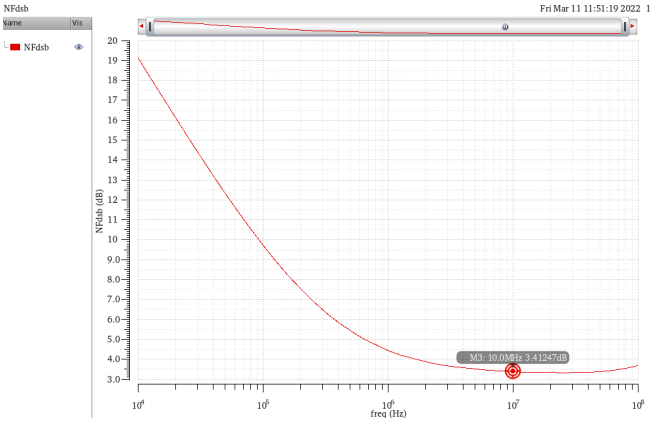


Fig. 21. Noise Figure Value of Upper Block Simulation

From the simulation results of NF (≤ 3.5dB), $IIP_3$ (≤ -10dBm), and Voltage Conversion Gain (≥ 30dB), the upper block satisfies the requirement of this receiver.

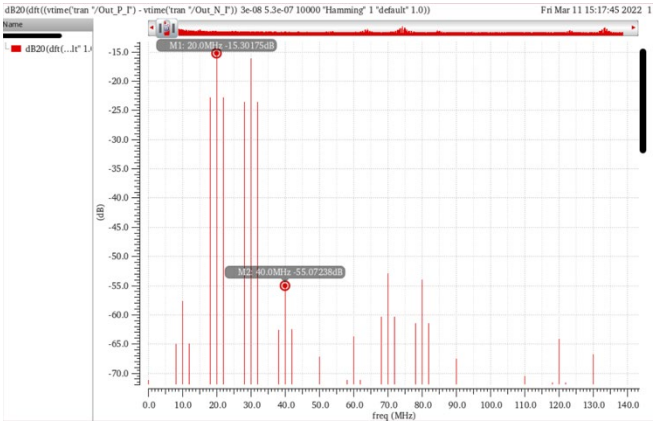


Fig. 22. $IIP_3$ Value of Upper Block Simulation

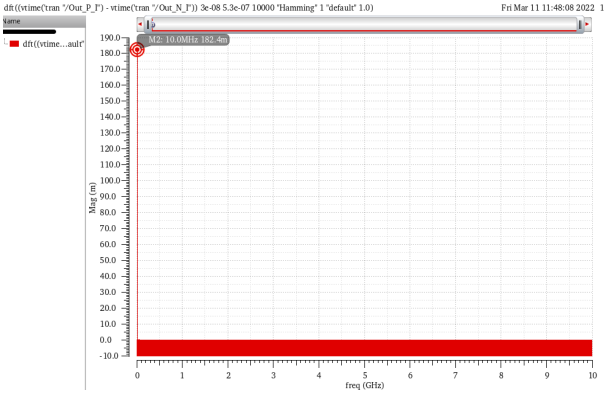


Fig. 23. Output Voltage Magnitude Value of Upper Block Simulation

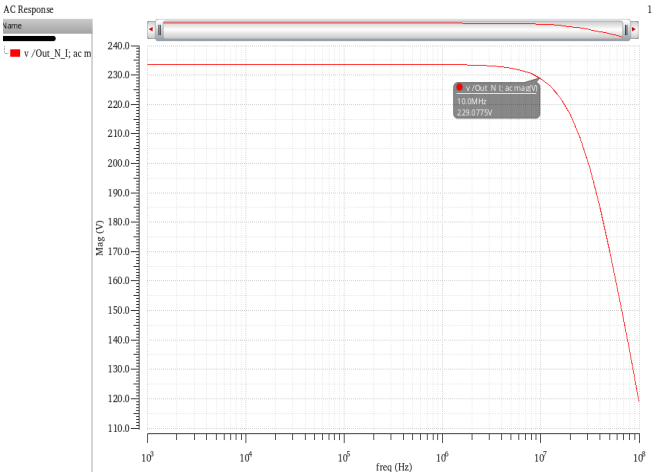


Fig. 24. Output Voltage Magnitude Value of Upper Block Simulation

## B. *Lower Block Simulation*

Figure 25 shows the circuit schematic of the lower block. In this block, we need to satisfy the requirements that phase noise of 5.2GHz LO < -110dBc/Hz at 1-MHz and also the output waveform should have the frequency of 5.19GHz

During the simulation process, we adjusted the parameters in the LO schematic. The finalized parameters are shown in Table VI in the conclusion part. Figures 26 to 27 show the simulation result of phase noise of 5.2GHz LO at 1MHz offset and output waveform frequency.

- Phase Noise at 1MHz offset = -111dBc/Hz
- Output Waveform & Spectrum Frequency = 5.19GHz

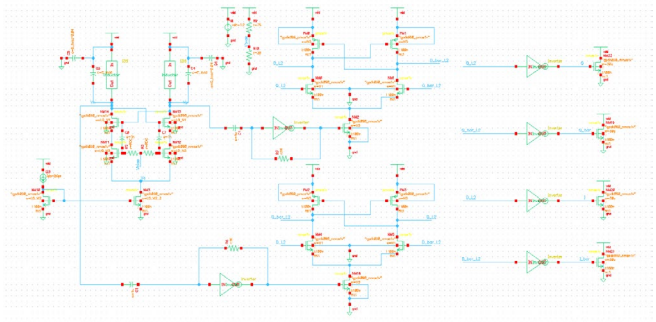

Fig. 25. Lower Block Circuit Schematic in Cadence

From the simulation results of PN @ 1MHz offset (≤ -110 dBc/Hz), and output waveform (at 5.19GHz), the lower block satisfies the requirement of this receiver.

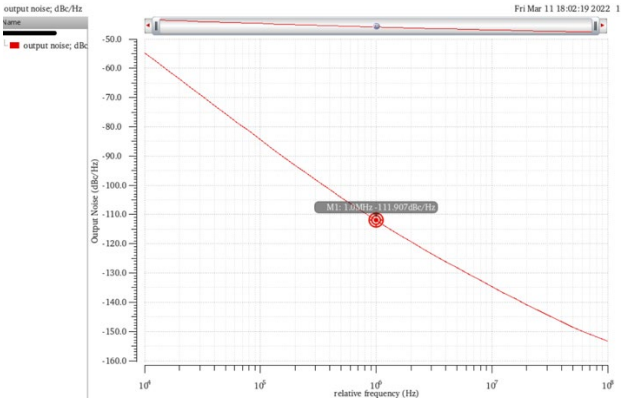


Fig. 26. Phase Noise Value at the 1-MHz offset of Lower Block Simulation

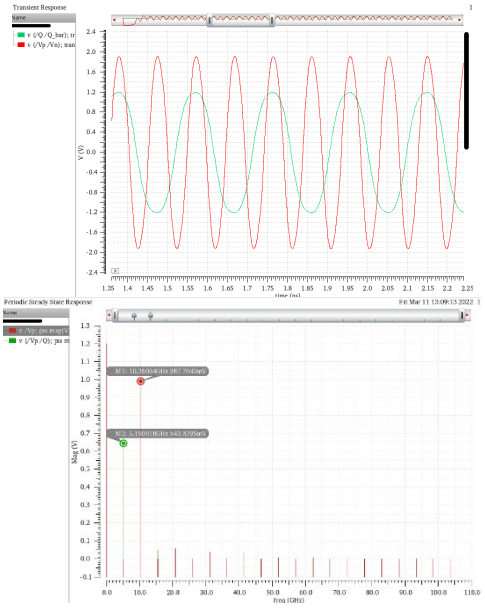

Fig. 27. Divide-by-2 Output Waveform and Spectrum of Lower Block Simulation (LO output in red – 10.38GHz & Divide-by-two output in green – 5.19GHz)

### C. *Overall Circuit Simulation*

To make the circuit view more straightforward to see the structure, we created symbols for all five blocks and combine them shown in figure 28.

However, there are some challenges during the overall circuit simulation. First, for NF simulation, since an ideal voltage source provides the upper part with frequency 5.19GHz in testing the upper block, we tried our best to achieve 5.19GHz exactly but failed (we get 5.19002GHz), which let us fail the simulation in pss and pnoise. Second, due to the same reason of ideal frequency and actual frequency, the IIP3 of the overall circuit is also being affected by the input waveform. To deal with this, we decided to use the NF of the upper part since, theoretically, the LO part will not affect the overall Noise Figure, which is dominated by the upper part.

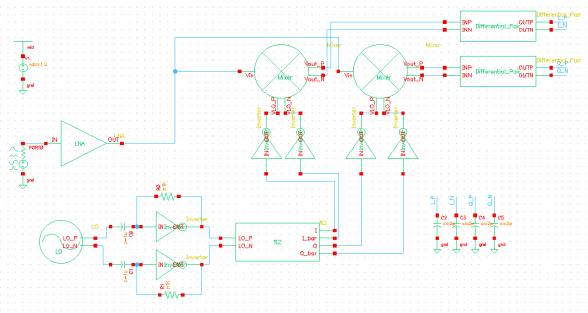

Fig. 28. Overall Receiver Design and Symbol Connection in Cadence

## VIII. PROJECT CONCLUSION

In summary, we finalized all our design parameters as shown from Table I to Table V and simulate all required performance values in Table VI.

TABLE VI. SIMULATION RESULT OF OVERALL RECEIVER

| Variable | $NF_{total}$* | $IIP_3$* | Gain | Phase Noise at 1MHz offset | $R_{in}$ | $R_{out}$ |
|---|---|---|---|---|---|---|
| **Requirement** | ≤ 3.5dB | ≤ -10dBm | ≥ 30dB | < -110 dBc/Hz | ≅ 50Ω | < 1000Ω |
| **Simulation Result** | 3.417dB | -10 dBm | 31.2 dB | -111 dBc/Hz | 50Ω | 229Ω |
| **Satisfied / Unsatisfied** | S | S | S | S | S | S |

For the value of $IIP_3$ and Noise Figure (as stared in Table VII), these two values result from the upper block due to the simulation limitation explained in the previous text.

In conclusion, all the performance and building-block specifications are satisfied. We used one current source for each block, and no DC voltages other than VDD are provided. Besides, we applied all inductors and capacitors using the required model with specific parasitic. The total inductance is 18.73nH, smaller than 100nH, thus fulfilling the requirement. By running, DC analysis, the total DC power of the receiver is 56.6mW.

## ACKNOWLEDGMENT

Our group gratefully acknowledge the technology support and circuit schematic design from the ECE215C class instructor, Professor Behzad Razavi, for providing the lecture material and textbook about each structure of the receiver and also the class teaching assistant, Yu Zhao, for providing the detailed simulation suggestion

## REFERENCES

[1] Tae-Sung Kim and Byung-Sung Kim, "Post-linearization of cascode CMOS low noise amplifier using folded PMOS IMD sinker," in IEEE Microwave and Wireless Components Letters, vol. 16, no. 4, pp. 182-184, April 2006, doi: 10.1109/LMWC.2006.872131.

[2] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, no. 9, pp. 835-841, Sept. 2001, doi: 10.1109/82.964996.

[3] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LANs," in IEEE Journal of Solid-State Circuits, vol. 34, no. 10, pp. 1382-1385, Oct. 1999, doi: 10.1109/4.792608.

[4] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998, doi: 10.1109/4.658619.

[5] Jafari, B., Sheikhaei, S. Phase noise reduction in LC cross-coupled oscillators using sinusoidal tail current shaping technique. Analog Integr Circ Sig Process 96, 125–132 (2018). https://doi.org/10.1007/s10470-018-1181-x