ELEC5280 Final Project Report

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***Abstract*—In the paper, a heterodyne receiver front end structure for 5G spectrum is presented, which down-converts the RF signal in the range of 27GHz to 29GHz down to 200MHz. The receiver front end consists of a 2 stage LNA, two mixers and followed by a VGA. The heterodyne receiver is able to provide 27.1 to 29.2 dB gain, at NF is 5.9dB, IIP3 is -14.1dBm, S11 is -14dB, while consumes 60mW.**

***Keywords*—receiver, LNA, quadrature mixer, VGA, 5G, 28GHz, CMOS.**

I. Introduction

A. Structure Overview

The heterodyne receiver is designed for centre frequency of 28GHz and Bandwidth is 27GHz~29GHz. Voltage Control Oscillator is used so that output IF frequency is fixed at 200MHz. LNA can reduce system Noise Figure and transfer single ended signal to differential ended signal. Then a low power downconverter Mixer will transfer RF frequency to IF frequency. This structure is depicted in fig 1. The cadence implementation of the whole receiver structure is shown in fig 2, with the name of each block labelled.

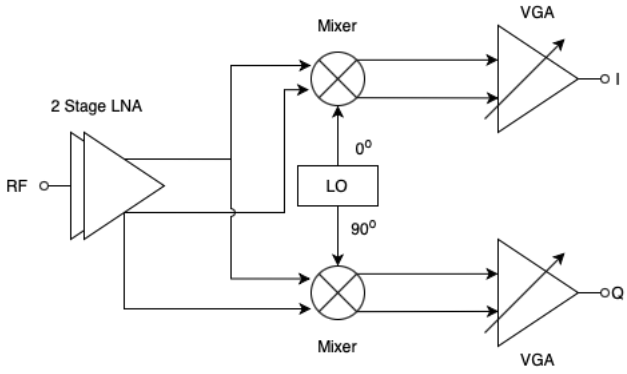

Fig 1. Proposed receiver architecture

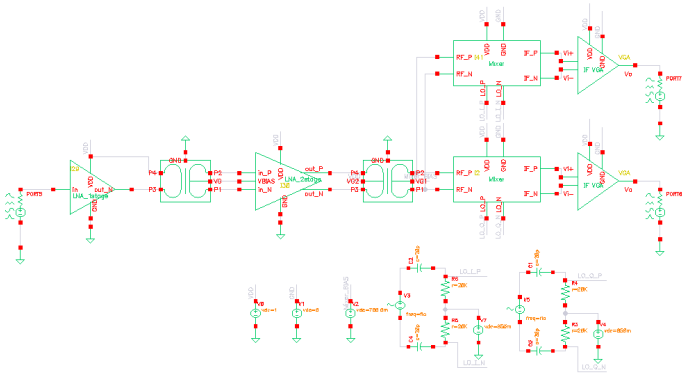

Fig 2. Cadence implementation of the receiver

B. Workload Distribution

	Guo Hao	Chen Runzhou	Ching Wai Kin
Design and Simulation of LNA	■		
Design and Simulation of Mixer		■	
Design and Simulation of VGA			■
Receiver System Simulation	■	■	■
EVM Simulation	■		
Report Writing		■	■

Table 1. Workload Distribution

Table 1 shows the Workload Distribution among our group.

II. Circuit Implementation

A. LNA Design

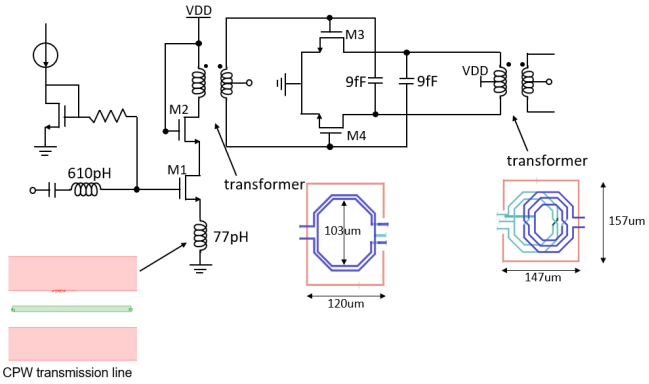

Fig 3. Proposed LNA schematic and transformer design

The LNA is designed to be 2 stage structure, as depicted in fig 3, to provide high gain to reduce the effect of NF from the succeeding stages. The first stage LNA is based on the conventional cascade structure, with transformer coupled output to convert single ended signal to differential. CPW transmission line is used due to the small value of source inductor. Second stage is a neutralized amplifier. The neutralized capacitor is added to eliminate effect of miller effect. The capacitance should be smaller than Cgd of the differential MOS to prevent amplifier self-oscillation. Table 2 shows the LNA performance.

	Values
Power Consumption	24mW
Voltage Conversion Gain	25dB
Noise Figure	2.7dB
IIP3	-1.5dBm
S11	-14dB

Table 2. LNA performance summary

Corner	Voltage Gain	Noise Figure	IP3
ss	27dB	2.9dB	-6.14dBm
tt	28dB	2.7dB	-5.89dBm
ff	29dB	2.6dB	-4.32dBm

Table 3. LNA corner simulation performance

B. *Mixer Design*

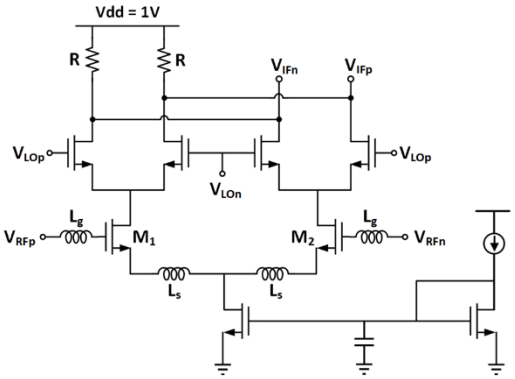

Fig 4. Proposed mixer schematic

The mixer design follows the design of Gilbert Cell, as depicted in fig 4. It produces output signals that are proportional to the product of two input signals. Such circuits are widely used for frequency conversion in radio systems. As a mixer, its balanced operation cancels out many unwanted mixing products, resulting in a "cleaner" output. Table 4 shows the mixer performance.

	Values
Power Consumption	4.9mW
Voltage Conversion Gain	1.08dB
Noise Figure	16.54dB
IIP3	3.75dBm

Table 4. Mixer performance summary

C. *VGA Design*

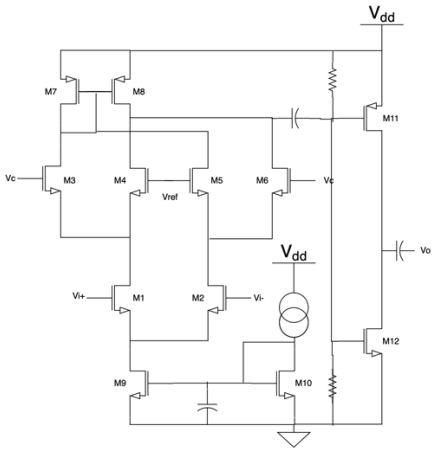

Fig 5. VGA schematics

The VGA is designed based on current steering structure to convert differential input to single ended output, with current mirror as an active load to ensure identical operation on the differential input, followed by single ended push-pull buffer stage, which output impedance can be tuned by the bias current to match any load at different impedance, as shown in fig 5. Table 5 shows the VGA performance.

	Values
Power Consumption	10.5mW
Voltage Conversion Gain	2-10dB
Noise Figure	12.5dB (low gain setting) 9dB (high gain setting)
IIP3	-17.7dBm
Bandwidth	1.2GHz

Table 5. VGA performance summary

III. Simulation Results

A. *Power Consumption*

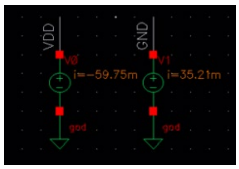

Fig 6. Current consumption at the VDD by DC analysis

Power consumption is simulated by DC analysis and the total power consumption is obtained by adding up current dissipation at each voltage source. From the result in fig 6 the total power consumption of all these sources mainly comes from the first one and its 59.75mW, smaller than 60mW, thus satisfying the requirement.

B. *Input Impedance & Matching*

To test the input impedance, SP analysis is employed. Results are shown in fig7 & 8.

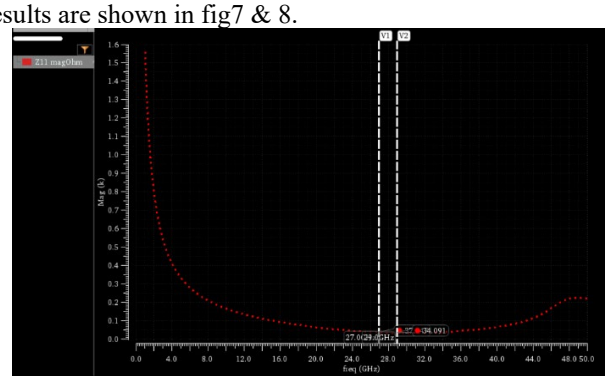

Fig 7. Simulation result of Z11

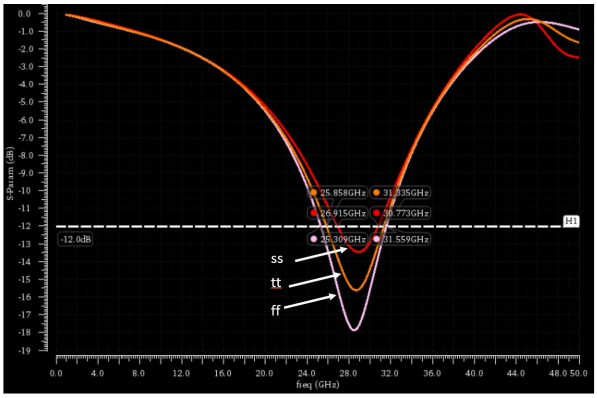

Fig 8. Simulation result of S11 [Three corner: ss & tt & ff]

Z11 ranges from 37Ω to 34 Ω with frf from 27GHz to 29GHz and equals to 35 Ω when frf = 28GHz. Therefore, the input impedance satisfies the requirement. The plot shows that S11 ranges from -14.35dB to -12dB in 26.2 to 31.4GHz frequency range. It is smaller than -12dB, thus satisfies the requirement.

C. Voltage Conversion Gain

To test the voltage conversion gain, PSS+PAC analysis are applied to compare VIF (at 200MHz) with VRF (at 27 – 29 GHz). In the PSS analysis, a beat frequency, Flo, is set for frequency down conversion, and the number of harmonics is set to be 2, such that, the result would cover entire frequency range of VRF. Simulation is shown in fig 9.

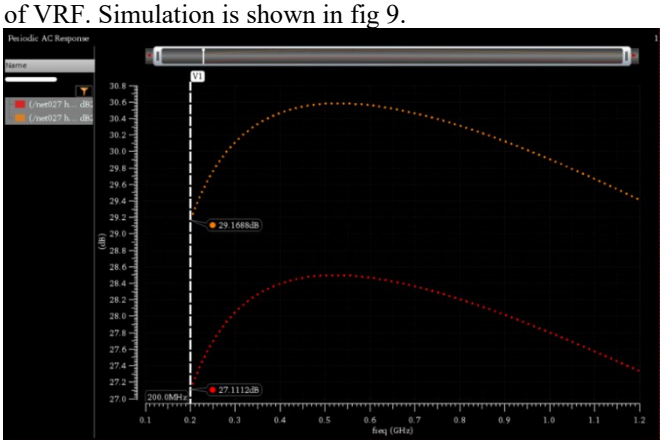

Fig 9. Simulation result of voltage conversion gain

Two tests were conducted for frf = 27GHz and 29GHz to prove that the gain is larger than 0dB for all frequency ranges. The plot is shown below. When frf = 27 GHz, the voltage conversion gain (shown in red curve) is 27.1dB > 25dB. When frf = 29 GHz, the voltage conversion gain (shown in pink curve) is 29.2dB > 25dB. Therefore, the voltage conversion gain satisfies the requirement.

D. Noise Figure

To simulate the noise figure, the RF source is changed to DC mode and PSS + PNOISE analysis were used. The setup of simulation and plot is shown below. The only fundamental tone is flo and the beat frequency is flo. The frequency range is set from 1M to 1G so that the IF is covered.

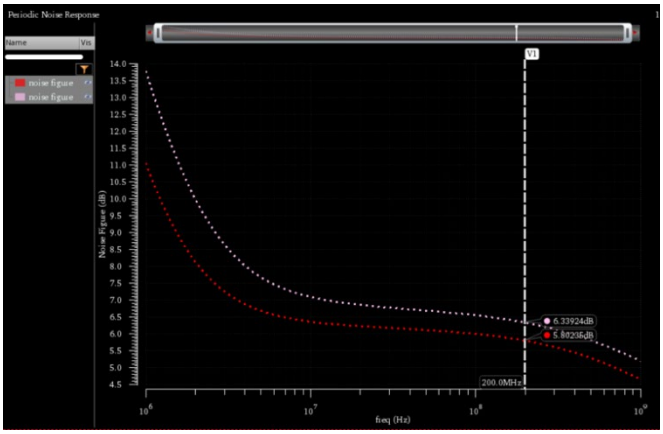

Fig 10. Simulation result of noise figure

Fig 10 is the plot of NF for frf = 27GHz (red) and 29GHz (orange) and the values are basically the same, which is around 5.8dB to 6.3dB at 200MHz, smaller than 7dB, which satisfies the requirement.

E. IP3

To simulate IIP3, HB analysis is applied. Since the input frequency is in the range of 27.5 to 28.5GHz, the IIP3 is simulated at two frequency setups, in order to test the performance through the entire RF range. The first setup is frf = 27.5 GHz and flo = 27.3GHz, with a 500MHz frequency separation for the two-tone test, another frequency frf2 = 28.0GHz is set in QPAC. The second setup is frf = 28.5 GHz, flo = 28.3GHz and frf2 =29GHz. Input power (prf) is swept from -50dBm to 20dBm with step size = 10. The extrapolation point is set to be -25 dBm.

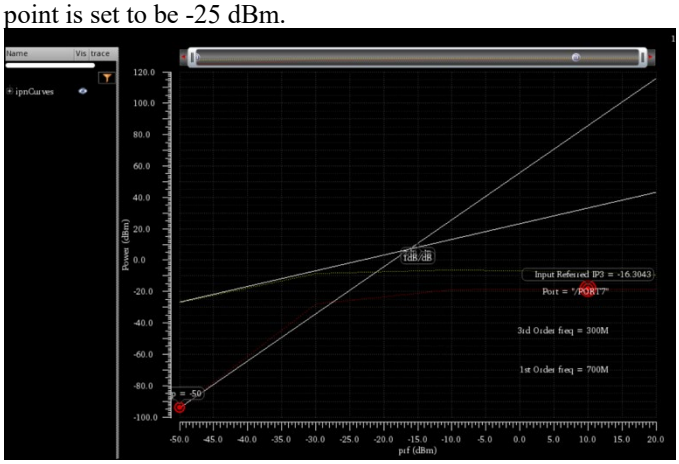

Fig 11. Simulation result of IIP3 at frf=27.5GHz & frf2=28GHz

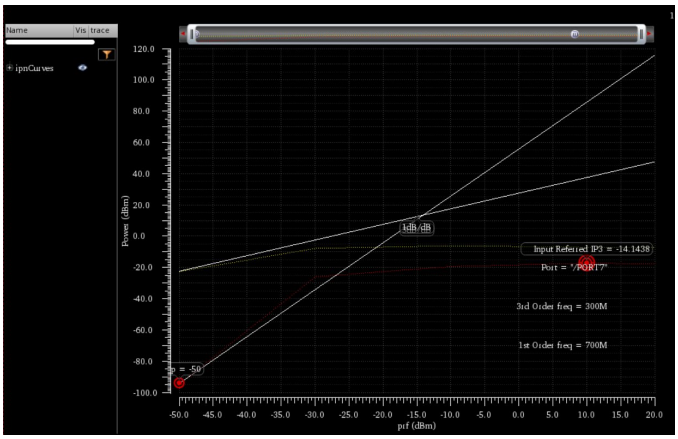

Fig 12. Simulation result of IIP3 at frf=28.5GHz & frf2=29GHz

Fig 11 shows the result of first simulation setup. Since the 1st harmonic = 28G – 27.3G = 700M, the parameter of flo is -1 and frf is 0, thus the 3rd harmonic = -1*(2*27.5G – 28G – 27.3G) = 300M, the parameter of flo is 1 and frf is -2. Then we select them and plot the IIP3. The result is -16.3dBm, larger than -20dBm, thus satisfying the requirement. Fig 12 shows the result of second simulation setup, resulting IIP3 is -14.1 dBm, which also satisfies the requirement.

F. *Transient Analysis*

Transient analysis is employed to examine the waveform at each port and the results are shown in fig 13. The waveform of RF input, Mixer input and IF input is as predicted. The LNA output has an envelope but it does not affect the outcome.

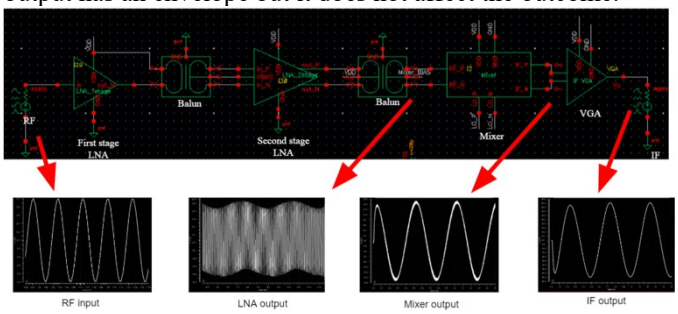

Fig 13. Simulation result of transient analysis

G. *Co-Simulation*

MATLAB, ADS and Cadence Co-simulation is employed to study the EVM of the proposed heterodyne receiver. The simulation result is shown in fig 14. The simulated EVM is 53.13%, which exceed the target value. Further study shall be taken place to reduce the EVM down to 10% to improve the BER and Package Error Rate before further development.

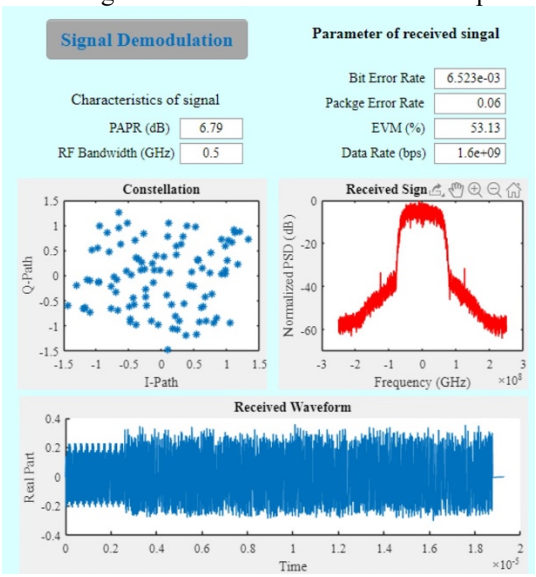

Fig 14. Simulation result of Co-simulation on EVM

IV. Performance Summary

	Calculated Results	Simulation Results	Requirements
Power Consumption	54.8mW	59.75mW	<60mW
S11	/	-14dB	<-12dB
Input Impedance	/	37Ω	50Ω
Voltage Conversion Gain	36dB	27.1 - 29.2dB	>25dB
Noise Figure	3.3dB	5.9dB	<7dB
IIP3	-17.7dBm	-14.1dBm	>-20dBm

Table 6. Overall performance summary

V. Conclusion

In this project, we designed a receiver at the transistor level to meet most of the specifications shown in Table. 6. The receiver is designed based on TSMC 40nm CMOS PDK and verified by OWL co-simulation platform. The three components: LNA, Mixer and VGA are designed based on the reference paper and most of the performance has met with the requirements, except the EVM. If we have opportunity to continue with this project, we would study the design consideration for better EVM and propose alternative structure to improve the EVM. All group members put a lot of effort and we learnt a lot about RF circuit design throughout this project.

References

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[2] C. Huang *et al*., "A CMOS 6-bit 16-GS/s time-interleaved ADC using digital background calibration techniques," JSSC, Apr. 2011.