EE215E Project Report

Runzhou Chen

Overall Link Performance

Metric	**SS Corner**	**NN Corner**	**FF Corner**
Data Rate[1] [Gb/s]	**6Gbps**	**8Gbps**	**8Gbps**
Eye Opening[2] [mV]	**152.2mV**	**107.7mV**	**127.2mV**
Offset LSB[3] [mV]	**2.0mV (Rx input) /2.5mV (Rx output)**	**1.6mV (Rx input) /2.5mV (Rx output)**	**1.3mV (Rx input) /2.5mV (Rx output)**
Offset Range [mV]	**16.3mV (Rx input) /20mV (Rx output)**	**12.9mV (Rx input) /20mV (Rx output)**	**13.0mV (Rx input) /20mV (Rx output)**
Average Power [4] [mW]	**29.5**	**29.8**	**30**

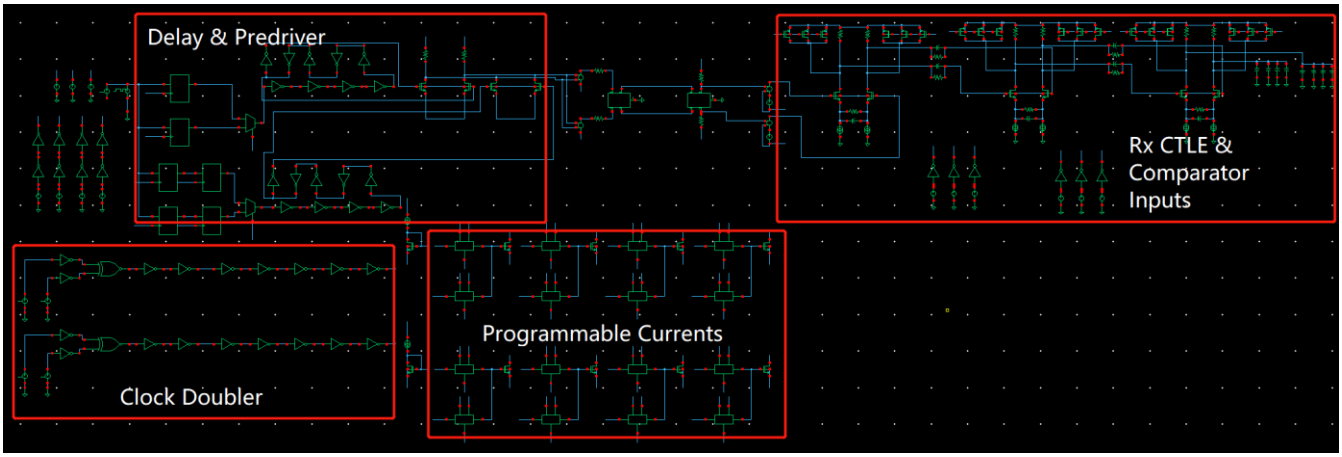
Design Energy Efficiency[5]

Component	**SS Corner [pJ/b]**	**NN Corner [pJ/b]**	**FF Corner [pJ/b]**
Tx Pre-driver/Driver	1.5×10^{-12}	1.5×10^{-12}	1.5×10^{-12}
Tx Buffer/Flip-flop	1.9×10^{-15}	7.4×10^{-16}	1.9×10^{-16}
Rx CTLE	2.18×10^{-12}	2.22×10^{-12}	2.25×10^{-12}

[1] Put the data rate at which all subsequent performance metrics for the given corner were obtained.
[2] Vertical eye opening, Peak-to-Peak (**not** the "box" method) measured at comparator inputs
[3] Make sure your report contains plots that demonstrate offset cancellation of both polarities, **over corners**.
[4] Obtain this metric by averaging the current draw from your VDD source over time.
[5] Add rows for your specific design components

Summary of the project

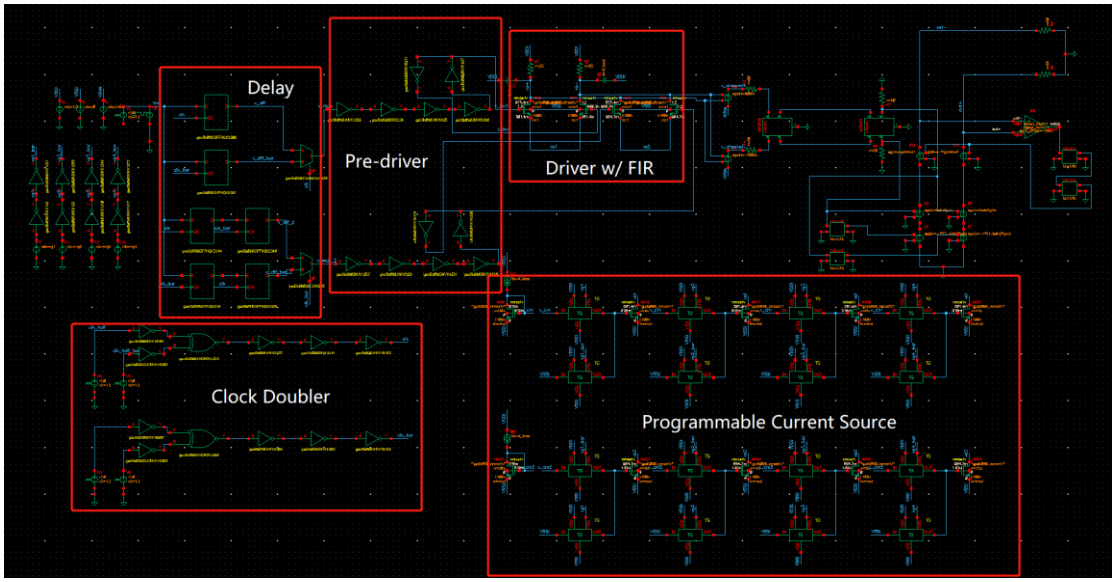
In this project, I design and simulate the transmitter, receiver, and any necessary equalization circuitry. Tx pre-emphasis and Rx CTLE are applied to reduce the ISI in order to reach the required 100mV eye-opening at the comparator. The whole circuit schematic is shown below.



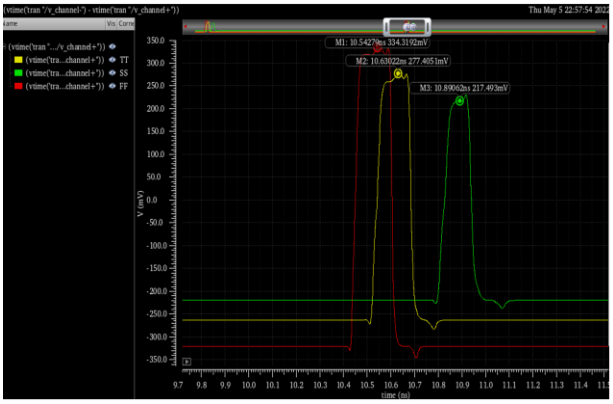
Part I. Tx Design

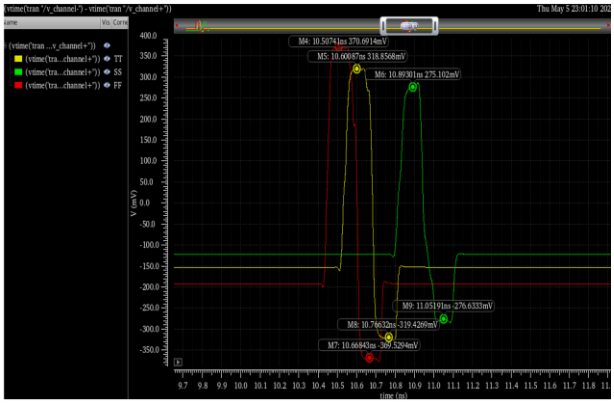
The target bit rate is set as 8Gbps.The Tx schematic is shown below and the design is as follows:

1. In order to have a dc swing of +/– 400mV i.e., each wire goes from Vdd to Vdd – 0.4V, I set the swing of the vprbs to be 200mV and a common DC voltage of 800mV at the input.
2. To implement the delay, I use DFFx4. According to the simulation, DFF cannot work at 8GHz clock so I use I/O channel with two 4GHz clock and a MUX to create an 8GHz bit flow.
3. Since only clock with frequency less than 3GHz are available, I use two 2GHz clock (I/O phase) and a XOR gate to achieve the frequency doubling. Extra inverter chain is used for large driving force and square waveform.
4. The pre-driver is designed to drive the CML driver. To achieve optimal fanout, a series tapered inverter is applied as the pre-diver. The first inverter has a size of x1 and each one that follows will have double size.
5. Tx Pre-emphasize is done by 2 CML driver: the termination resistor is 25ohm to mimic the real case. The switching MOSFETs have large size to model the ideal switch. I applied 2-tap FIR at Tx: b[n] = (1-a) d[n] + ad[n-1]. After iteration I set the parameter a = 0.7 for optimal performance.
6. The 50% programmability is realized by current mirror to minimize PVT variation. Suppose the total current is I and we have a = 0.7, 50% programmability means from 0.3 to 1.0. Then we use 3 digits to cover the range from 0.3 to 1.0 (times the total current) and assign those bits to corresponding MOSFET widths. The MOSFETs are powered by current mirror and can be turned on or off by self-made transmission gates. E.g., if we want to assign 0.7 to d[n] and 0.3 to d[n-1], then the control bit should be 100.

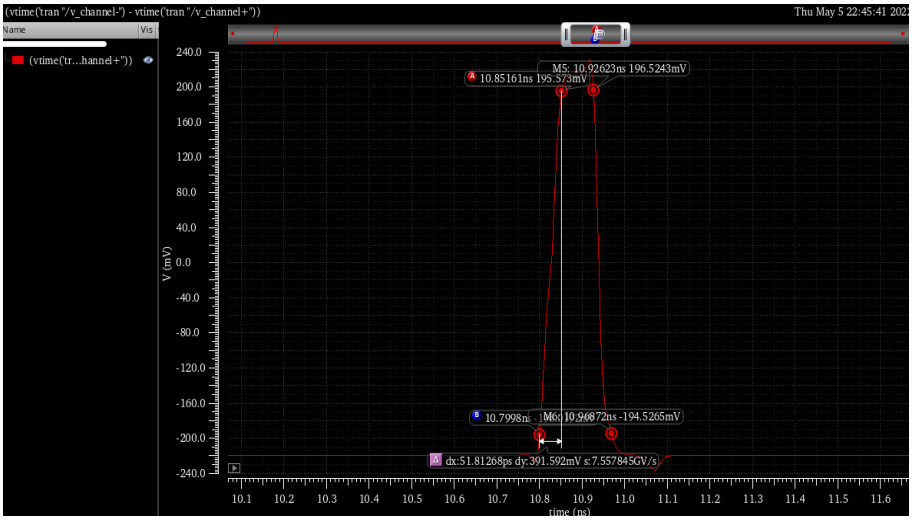


7. The pulse response before (above) and after (below) equalizations with TT, FF and SS (75% frequency) corners are shown below, we can see that after equalization, the delayed pulse has a negative value and the amplitude of the first and the second pulse is 7:3, the same as the FIR coefficient.





8. Slew rate check: we take the slowest corner (SS) and measure its rise and fall time. The total rise time is 51ps and fall time is 43ps. Since I'm using 6GHz, $\frac{T_{bit}}{3}$ is 52ps. Thus the SS corner satisfies the slew rate and other corner should also satisfy it.



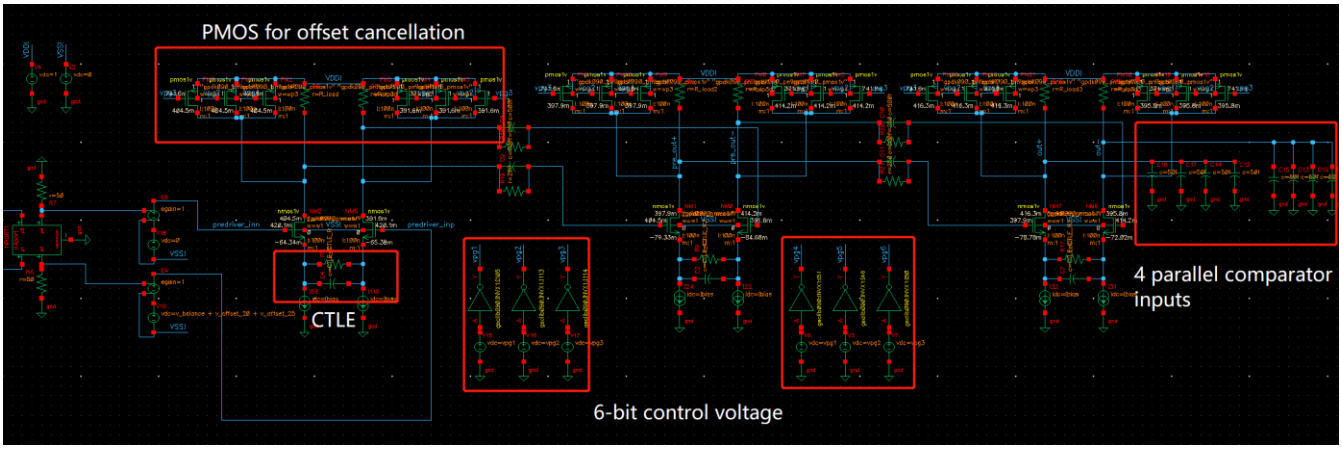
Part II. Rx Design

The target bit rate is set as 8Gbps. The Rx schematic is shown below and the design is as follows:

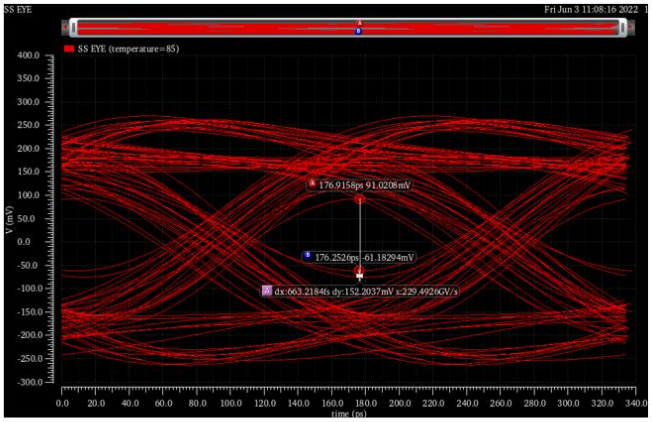
1. In Rx, a 3-stage CTLE is applied to achieve 1+az^-1, where a is 0.25. According to the transfer function, the poles and zeros can be found as:

$$\omega_z = \frac{1}{R_s C_s}, \omega_{p1} = \frac{1 + 0.5gmR_s}{R_s C_s}, \omega_2 = \frac{1}{R_D C_{load}}.$$

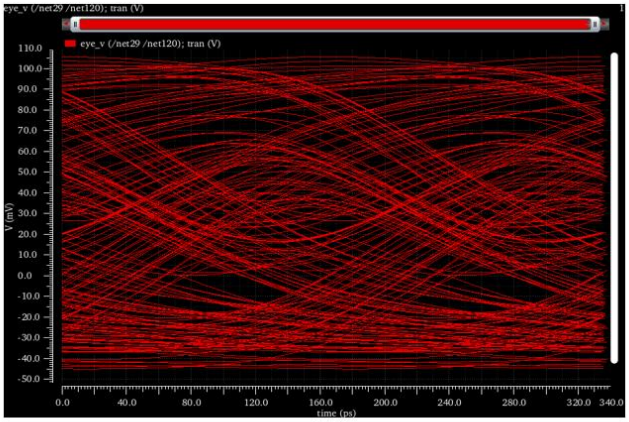
2. Then we choose Rs = 100ohm, Cs = 1.2fF, RD = 153ohm, Id = 4mA for the pre-driver to get the desired transfer function.
3. At the output, we place 3 PMOS at each side for offset cancellation with 6-digit control. The 3 PMOSs with width of 725nm, 500nm and 100nm are controlled by 3 digits. Once one of them is turned on/off, the current flows through the load resistor will change according to KCL. The DC offset from +/– 20mV to +/– 2.5mV can be cancelled.
4. To model the comparator input, we put 4 parallel 50fF capacitance for 4 paths.



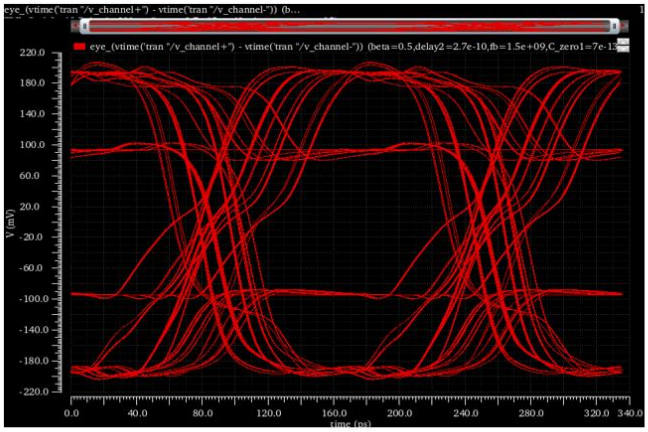
SS corner eye diagrams:



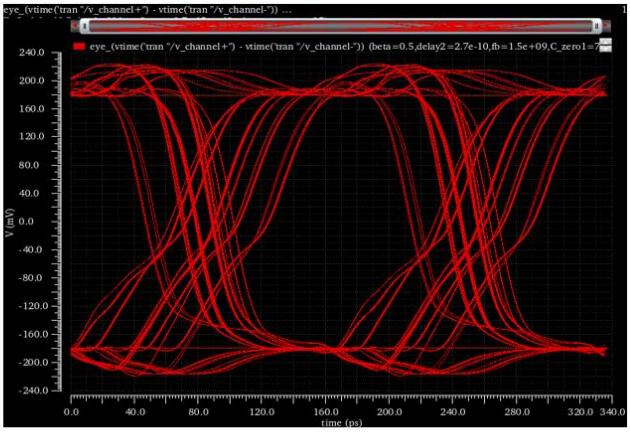
SS corner comparator input with equalization



SS corner comparator input without equalization

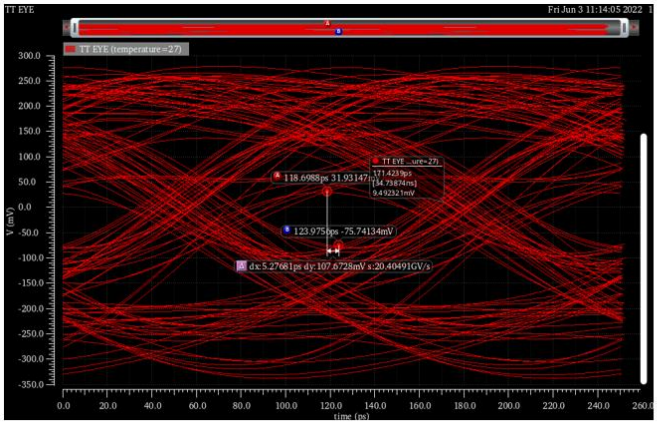


SS corner Tx input with equalization

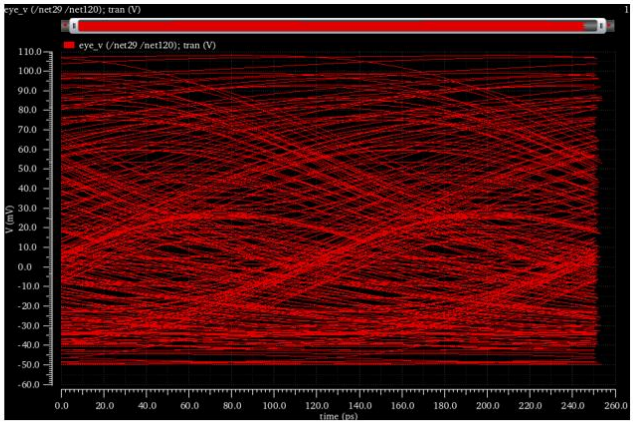


SS corner Tx input without equalization

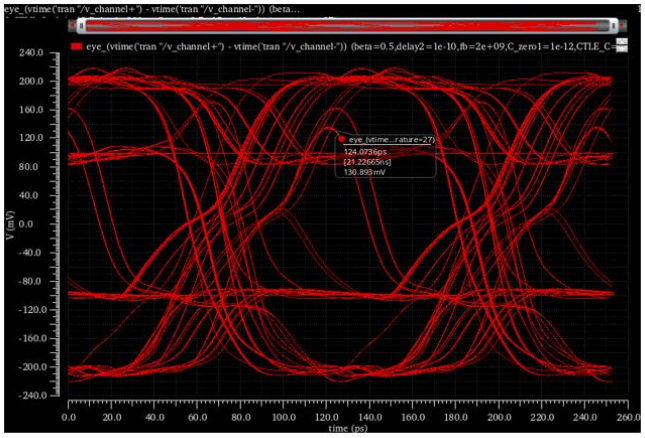
TT corner eye diagrams:



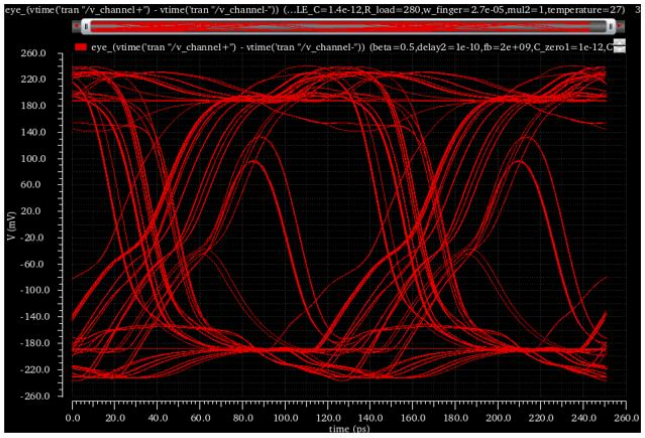
TT corner comparator input with equalization



TT corner comparator input without equalization

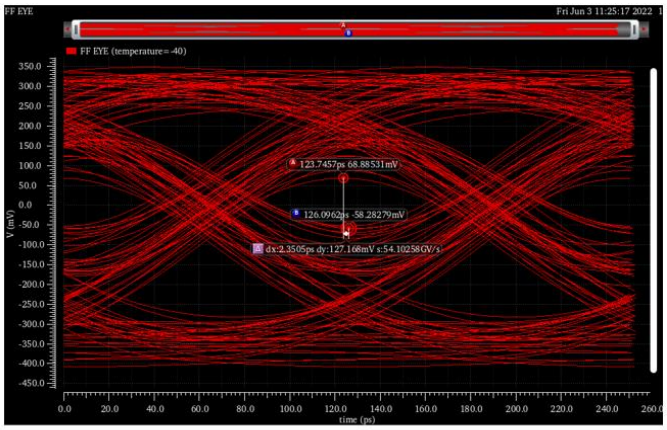


TT corner Tx input with equalization

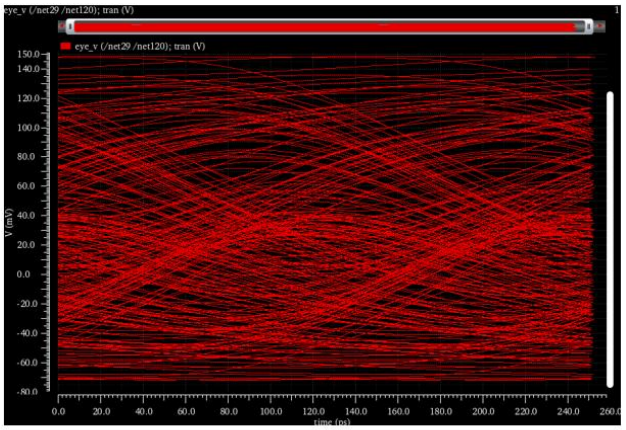


TT corner Tx input without equalization

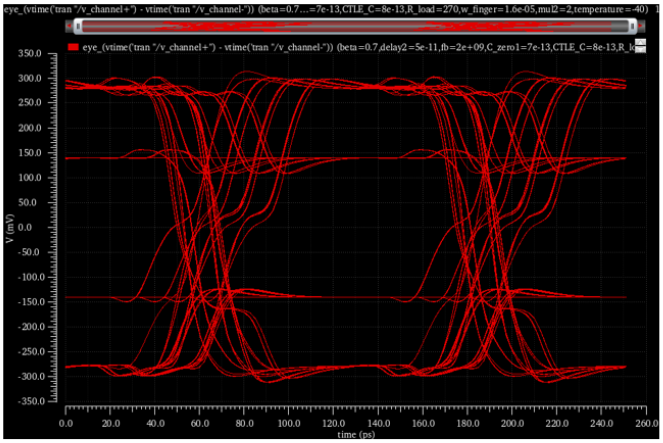
FF corner eye diagrams:



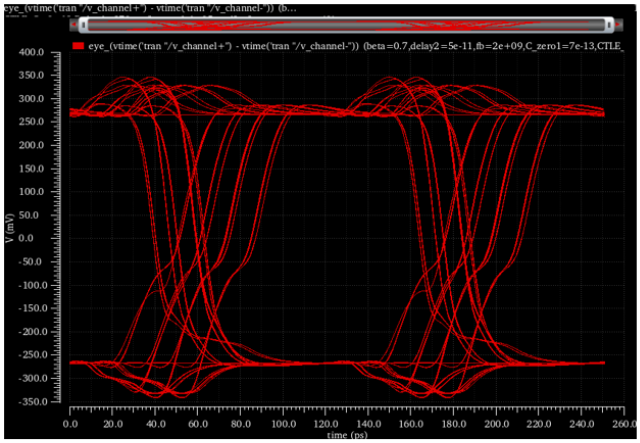
FF corner comparator input with equalization



FF corner comparator input without equalization



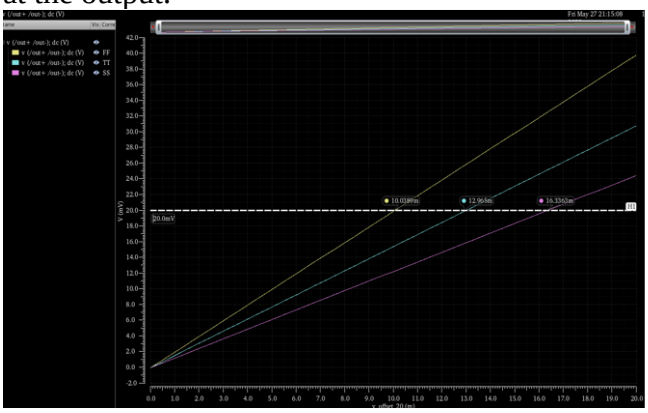
FF corner Tx input with equalization

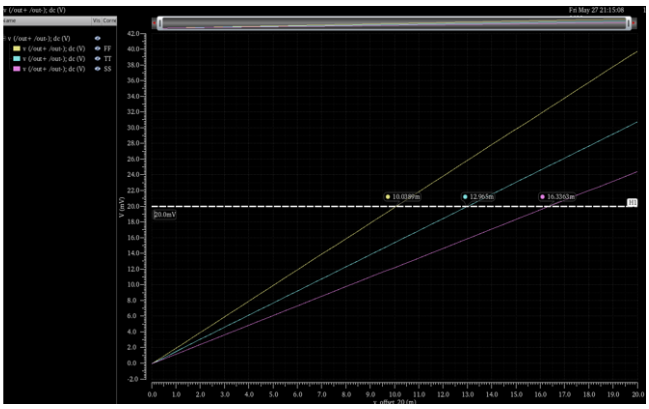


FF corner Tx input without equalization

SPart III. Rx CTLE Offset Cancellation:

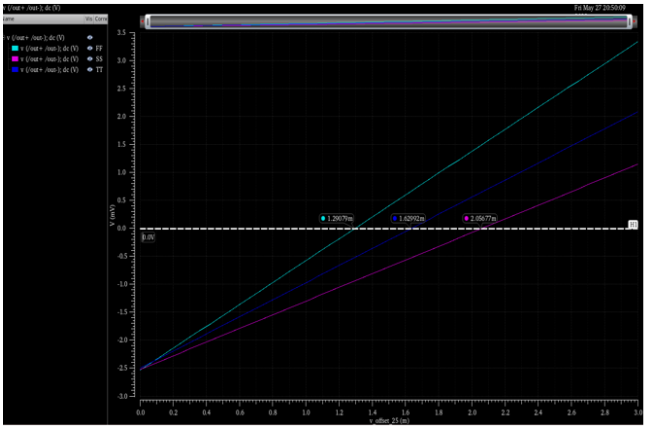
we first apply appropreate voltages at the pre-amplifer input to create output offset of +/– 20mV, +/– 2.5mV at the comparator input. We see below that the input-referred offset should be +/– 1.29mV, +/– 1.63mV and +/– 2.06mV for FF, TT and SS corners. Then we change the width of the PMOSs so that when the control digit: 000001 is assigned, the 2.5mV offset can be cancelled at the output.



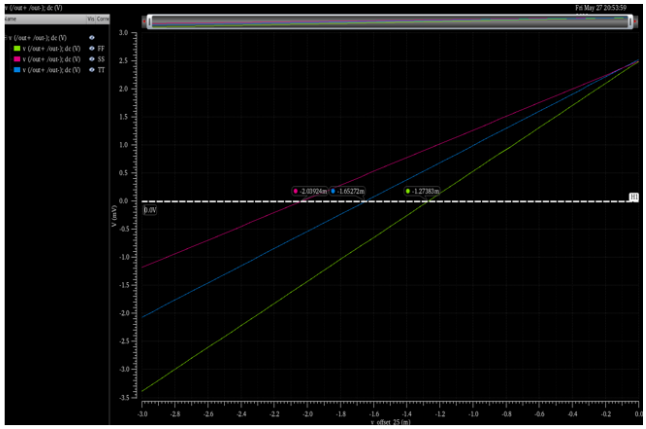


Next we repeat these steps for 20mV offset. See below that the input-referred offset should be +/– 10.24mV, +/– 13.13mV and +/– 16.43mV for FF, TT and SS corners.Then we change the width of the PMOSs so that when the control digit: 10000 is assigned, the 20mV offset can be cancelled at the output.

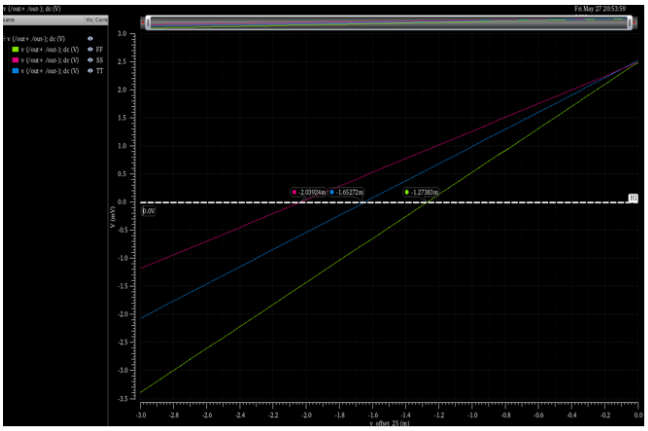
Then we plot the differential DC voltage at the pre-amplifier output (comparator inputs) with your offset cancellation circuitry included, versus the swept voltage at the pre-amplifier input. When the differentially applied input voltage (x-axis) reaches the input-referred offset value you are demonstrating cancellation of, the differential output voltage is zero.



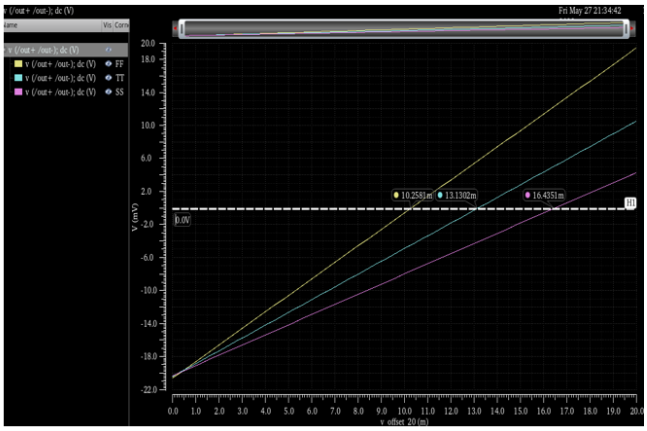
Output offset vs Input (2.5mV)



Output offset vs Input (-2.5mV)



Output offset vs Input (20mV)



Output offset vs Input (-20mV)