EE279AS Final Project

A 200-GHz PA with 40-dB Bandwidth and 10-dBm Psat

Runzhou Chen Christopher Chen

	Midterm Project	Final Project Spec	
Small-Signal Gain (@200GHz)	20.34dB	20dB	
3dB Bandwidth	160-223GHz	180-220GHz	
PAE	5.6%	10%	
S11 (across BW)	<-15dB	<-10dB	
S22 (across BW)	<-8dB	<-10dB	
Psat	3.775dBm	10dBm	
Stability	K, μ>1	K, μ>1	

I. Midterm Project Results and Final Project Specifications:

From the table above, we can see that we need to focus on improving the PAE and P_{sat} of our amplifier, as well as getting a better output matching. Of these parameters, increasing P_{sat} is the easiest since we could put multiple stages in parallel and use a Wilkinson power divider to combine the power at the output. The output matching (S22) could be achieved by adjusting the lengths of the transmission lines at the PA output, with some impact on the gain. However, in order to increase the PAE, we need to go back to optimize every stage of our amplifier.

II. Three-Stage PA Design:

A. T-Line Loss:

Similar to the midterm project, all transmission lines were modeled to have a 0.4dB loss per 90° of line at 200GHz with a substrate dielectric constant of 4. The attenuation factor is set to be 2262 according to the calculation.





B. Topology:

For the final project, we first focused on optimizing the topology that we used for the midterm project in order to improve our PAE. The topology consists of two cascode stages for gain, followed by a single common emitter stage for maximum power delivery.

Once we had optimized the three-stage PA to have sufficient gain, matching, and PAE, we planned to use a Wilkinson power divider in order to combine N number of PAs in parallel to boost our Psat to meet the project spec.



For the final project we used the same schematic as we did in the midterm project. The reason is that, according to the ideal case testing, a single stage common-emitter amplifier can provide a voltage gain as large as 5-6dB while a single stage cascode amplifier can provide 8-10dB gain. Therefore, if properly tuned, the 3-stage structure (two cascades and one common-emitter) are promised to render a gain higher than 20dB. In addition, our simulation in the midterm project indicated that only PAE and Pout needed to be improved. Therefore, we stuck to our original design.

The first two stages are used for boosting the voltage and power gain, the last stage is for high output voltage swing and to prevent the whole circuit from instability. To improve the output power (also PAE), the multipliers of the 2nd and 3rd stage are increased to 7 and the bias voltages are adjusted accordingly.

III. Three-Stage PA Results *A. S-Parameter* The amplifier is well-matched at 200GHz (S11 = -21.297dB and S22 = -14.79dB). The reverse isolation (S12) is -46.036dB, while the gain (S21) is 20.921dB. Across the project bandwidth (180-220GHz), the S11 and S22 are less than -10.344dB and -13.247dB, respectively.



B. Related Formulas



C. Voltage Gain and Psat

The measured small-signal gain is 20.92dB. The P1dB is around -13dBm. Plotting the Pout vs. Pin curve, the P_{sat} is 10.365dB. Both values can satisfy the requirement.



D. DC Power

The DC power (in W) was calculated by adding the total power from all independent sources (bias voltages and VDD).









F. Stability

Both the K-factor and Mu of the amplifier are greater than 1Hz to 400GHz, showing that the amplifier is unconditionally stable.



$G.P_{IP3}$

Plotting the power of the first and third harmonic across input power, the IP3 of the amplifier could be extracted. The OIP3 is 27dBm and the IIP3 is 7dBm.



G. Additional Figures

Plotting the output transient waveform, we can verify that the amplifier is indeed stable and not oscillating. The harmonic balance spectrum when Pout is 0dBm is shown below.



III. Power Combining Design

From the previous results, we can see that we were able to achieve all the specs for the final project with just a three-stage amplifier. However, we also designed a simple 2-to-1 power combining network with a Wilkinson power divider in order to compare the performance.

A. Wilkinson Power Divider

The Wilkinson power divider was designed based on the dimensions and parameters discussed in class.



From the s-parameter plots, we can see that the designed power divider has good matching at both the input and output ports, as well as good isolation between the two output ports. Because the power is split equally between the two ports, the ideal S21 and S31 should be -3dB. From the simulations, we see an additional

0.52dB of loss from the lossy transmission lines and resistor. The input and output s-parameter plots are shown below. Since both output ports (port 2 and port 3) are symmetric, only port 2 results are shown.



B. Power Combining

Using the Wilkinson power combiner and the three-stage PA discussed previously, a 2-to-1 power combining network was simulated without any optimization.



The detailed the 2-to-1 power combining PA schematic is shown below.



IV. Power Combining Results

A. S-Parameters

The amplifier input matching at 200GHz degrades a bit (S11 = -17.909dB and S22 = -15.023dB). The reverse isolation (S12) is -45.848dB, while the gain (S21) is 19.51dB. Across the project bandwidth (180-220GHz), the S11 and S22 are less than -9.872dB and -14.151dB, respectively. The degradation in the gain and input matching could be because of imperfect matching and isolation between the Wilkinson power divider and the three-stage PA's, so that each path sees an additional loading effect.



B. Voltage Gain and Psat

The measured small-signal gain is 19.509dB. The P1dB is around -8dBm.



Plotting the Pout vs. Pin curve, the P_{sat} is 12.814dB.

As expected, the P_{sat} of the combined structure increased by about 2.5dB and the P1dB also increased.

C. DC Power

The DC power (in W) was calculated by adding the total power from all independent sources (bias voltages and VDD). As expected, the total DC power of the combined structure is twice that of the three-stage PA since there are two in parallel.



D. Efficiency

The peak PAE is measured to be 10.5%. The peak drain efficiency is slightly higher at 11.1%.



The efficiency of the combined structure is Sslightly degraded, which can probably be attributed to the imperfect matching of the PAs with the Wilkinson power divider, leading to additional loading from the parallel PA.

E. Stability

Both the K-factor and Mu of the amplifier are greater than 1Hz to 400GHz, showing that the amplifier is unconditionally stable.



 $F. P_{IIP3}$

Plotting the power of the first and third harmonic across input power, the IP3 of the amplifier could be extracted. The OIP3 is 33dBm and the IIP3 is 13dBm.



V. Conclusion

A. Comparison

Comparing the three-stage PA on its own with the combined structure, we can see that there is an increase in the P_{sat}, P1dB, and IP3 values, as expected. However, the gain, input matching, and efficiency all dropped. We believe this may be because of the imperfect matching and isolation of the two parallel PA's with the Wilkinson power divider. With additional tuning, these metrics should be able to be improved to match our performance of the uncombined structure. However, since the uncombined structure can achieve sufficient performance to meet the final project specs, we decided not to spend any time optimizing the combined structure.

	Final Project Spec	Three-Stage PA	Power Combining PA
Small-Signal Gain (@200GHz)	20dB	20.9dB	19.5dB
3dB Bandwidth	180-220GHz	107-241GHz	103-245GHz
PAE	10%	12%	10.5%
S11 (across BW)	<-10dB	<-10.3dB	<-9.8dB
S22 (across BW)	<-10dB	<-13.2dB	<-14.2dB
Psat	10dBm	10.4dBm	12.8dBm
Stability	K, μ>1	K, μ>1	K, μ>1
P _{IIP3}	/	7dBm	13dBm

B. Results Summary Table