A 2-GHz Class-B Power Amplifier on GaN-Based HEMTs

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***Abstract*—A 2-GHz two stage Class-B power amplifier with optimized load and balanced architecture is designed and evaluated in this report. The proposed power amplifier is designed on GaN based HEMTS. The proposed power amplifier is designed in balanced architecture with two branch-line couplers to realize S11&S22 below -20dB. The bias is chosen properly to achieve a Class-B operation with a decent Power Added Efficiency(PAE) of 55%. Additionally, a gain of 28.3 dB is reported in this design using two stage cascaded structure. Load pull is employed to get a maximum output power of 45.7dBm. The power bandwidth is calculate to be 600MHz**

***Index Terms*—Branchline Coupler, HEMT, Power Amplifier, Load pull, Class-B, ADS, Matching Network.**

I. Introduction

POWER amplifiers are critical devices that have been widely used in modern wireless transmitter techniques where power amplifiers are usually designed to amplify small data signal while maintain good signal quality. Gain, stability, power efficiency and maximum output power are key specifications in power amplifier design. The power amplifier bias is chosen to be Class-B operation for decent efficiency. Considering that a single stage amplifier does not provide sufficient gain, a two stage structure is utilized for high gain. Also, two branch-line couplers are added to absorb the reflected power while terminating the third harmonic to guarantee a pure output spectrum. Most importantly,load pull simulation is performed to boost the output power.

This report is organized as following: Section I describes the device performance simulations including bias optimization for Class-B operation, load pull determination for maximum output power and stability. Section II introduces the input/output matching network and a single stage amplifier results. Section III discusses about the two stage cascaded power amplifier and the balanced architecture design with layout integration. Section IV presents all the simulated results in details.

A. Subsection Heading Here

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II. Transistor Performance Simulation

To choose the proper DC bias for the transistor, we referred to the CGH40010F datasheet in which we found that the gate threshold voltage is around -3V and is 28V [1]. Then we performed the load-line analysis to find out the specific bias point that renders class-B operation for the transistor. Using the display template provided by Keysight, we swept the drain and gate voltage and plotted its load-line and V/I waveform [2]. In Fig. 2 we see that the transistor output has a 180-degree conduction angle, which guarantees a class-B operation.

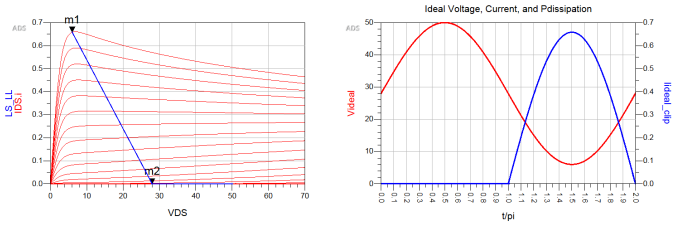

Fig. 1. Load line simulation

The stability characteristic of the HEMTs is performed using ADS load-line template and the it shows that the transistor is not stable below 1.5GHz. A 10 Ohm resistor is added at the gate of the transistor to guarantee an unconditional stability across the interested frequency band. Ideally, adding another large shunt resistor at gate would further enhance the low-frequency stability but this is omitted here.

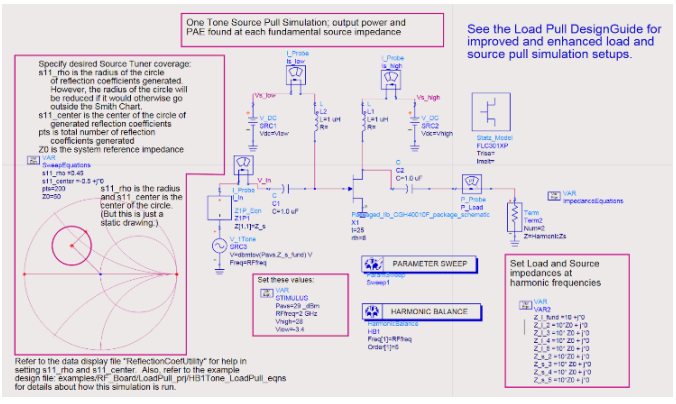

Fig. 2. Loadpull simulation setup

Load-pull is often applied to find the optimal load impedance of the transistor to deliver the maximum power. Similarly, source-pull is for the optimal source impedance. The simulation step-up in ADS using Load/Source pull template is shown in Fig. 2. In the load-pull and source-pull template we plugged in the transistor and its 10-ohm stability gate resistor and ran the simulation. Similar steps were applied

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Manuscript finished December 9, 2022.

to the source-pull. To have the maximum output power, we should set the source and load impedance to be:

$$Z_{opt-load} = 19.2 + j2.8 \tag{1}$$

$$Z_{opt-source} = 6 + j0.03 \tag{2}$$

III. Single Stage Amplifier Design

In section II.C we concluded that the optimal load and source impedance are given by 19.2 + j2.8 ohm and 6 + j0.03 ohm. To match the output impedance to 50-ohm port, we calculate the quality factor to maintain relatively wide bandwidth:

$$Q = \sqrt{\frac{R_{load}}{R_{load}} - 1} \tag{3}$$

For a better bandwidth, we designed a 2-stage L-section matching network consists of lumped elements. The shot-stub can also be viewed as a DC-feed and connect to the gate bias voltage. The design was realized in the Smith Chart tool in ADS and is shown in Fig. 3. Similar design methodology was applied to the output matching network and we added DC-blocking capacitors to block the DC voltage at both input and output. Some modifications were made to simplify the matching network.

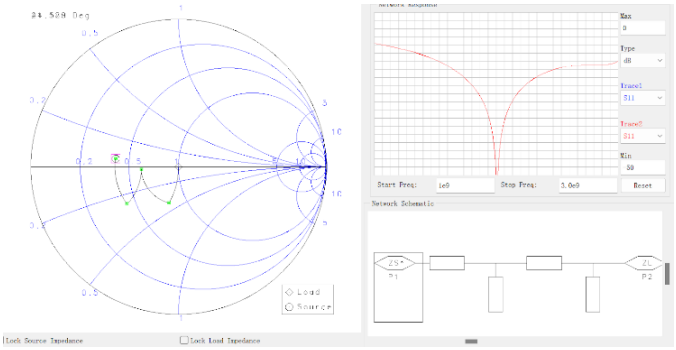

Fig. 3. Matching Network Design

To verify the matching network design, we tested the single-stage amplifier circuit. We applied S-parameter and Harmonic Balance analysis with the display template provided by Keysight to demonstrate the harmonic rejection [2]. The single stage amplifier schematic and simulation results are shown in Figure.4 and Figure.5, respectively.

As shown in Figure.5, the single transistor can achieve a 12.9-dB power gain with 1.3-GHz bandwidth and excellent input matching $S11 \leq -40\text{dB}$ and harmonic rejection above 35dB. This proves that the matching circuit design is successful.

IV. Two Stage Power Amplifier Design

To boost the overall power gain, we decided to build a 2-stage amplifier that was expected to realize a gain higher than 24dB. The first step was to deign the inter-stage matching

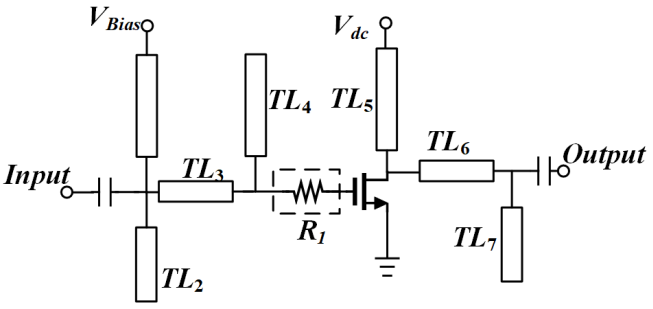

Fig. 4. Single Stage schematic of Power amplifier

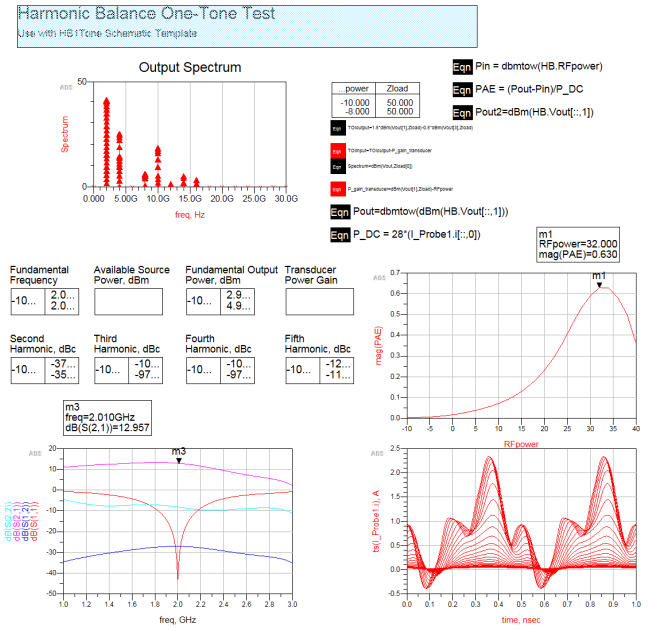

Fig. 5. Single Stage simulation results

network that matches the optimal source and load impedance while minimizing the loss. The design should contain 2 DC feeds for 2 DC bias (the drain bias for stage 1 and the gate bias for stage 2) and 1 DC block to separate the drain and gate voltages. Two methods were tested and are shown in Fig. 6. The first method uses a coupled-line coupler that serves as 2 DC feeds and 1 DC block, then the requirements are directly met. The second method is straight-forward and uses 2 transmission lines are DC feeds and a capacitor as DC block. After testing the second approach was chosen due to less layout difficulty and corresponded loss. The circuit diagram for the 2-stage amplifier is shown in Fig. 6. The input, output and inter-stage matching are based on the designs mentioned in the previous sections. We used the same template as in the single-stage amplifier. The power gain is doubled to 25.9 dB while the bandwidth and input matching remains unchanged. We also observed a degradation in 2nd harmonic rejection and PAE (63% for the 1-stage and 53% for the 2-stage amplifier). These will be improved in the later sections using balanced structure.

Advantages of balanced Amplifier: in/out matching, har-

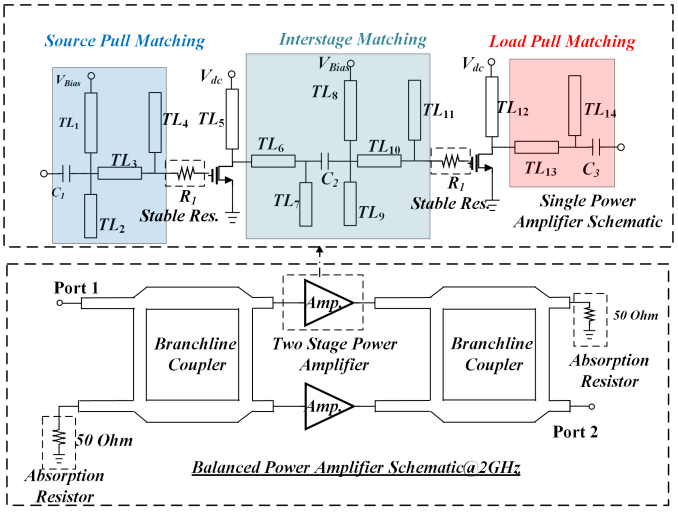

Fig. 6. Circuits diagram of the proposed power amplifier

monic rejection, etc.

To realize a balanced power amplifier, 90° branch-line couler should be added at both input and output. As shown below, the branch-line S-parameter shows that each coupler will lead to a 90° phase shift at fundamental harmonic while -90° phase shift for 3rd harmonic at two output ports which eventually combines the fundamental harmonic at output port and absorbs the 3rd harmonic at terminating resistor to purify the spectrum.

$$S_{parameter} = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{4}$$

Another important design consideration for ° branch-line coupler is that the reflected wave from mismatch of transistor input/output will eventually come to terminating load instead of input/output port which guarantees good input/output S-parameters. The simulation results of the hybrid coupler is shown below with return loss lower than -25dB and amplitude imbalance 0f 0.3dB.

Using the hybrid coupler to connect two 2-stage amplifiers

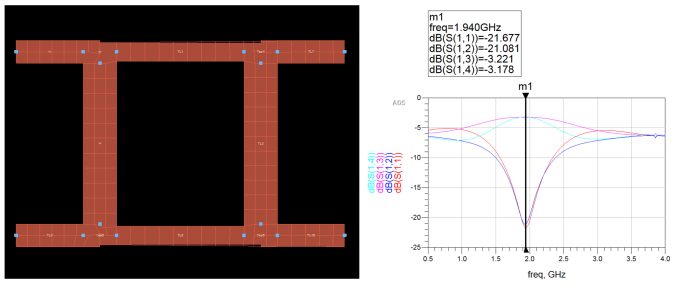

Fig. 7. Topology and simulation results of hybrid coupler

in the last section, we have the circuit diagram for the balanced amplifier as shown in Fig. 6. Using the same template as in the previous amplifiers, the simulation results are displayed in Fig. 7. It can be observed that both input and output matching bandwidth are improved significantly with the help of the hybrid coupler. The current waveform shows a clear cut at around 0A which corresponds to the class-B operation. For the PCB board we selected Rogers 4003c whose datasheet and ADS substrate set-up are explored. The thickness is 1.5mm, the dielectric constant is 3.38 and the loss tangent is 0.0021.

To convert the lumped elements to layouts, we first replaced each ideal transmission line with the real microstrip element. The substrate parameter is given in the previous section and its physical width and length can be calculated based on its characteristic impedance and electrical length using LineCalc in ADS. Then for the connection between microstrip lines, we added T-junctions for the short stubs and some extra microstrip lines at the input and output to avoid direct connection between T-junctions and wires, which would cause problems in post-layout simulation.

The next step is to generate the layout using the Layout tool in ADS. Careful arrangement of elements can reduce the loss compared to the ideal components.The circuit diagram with all transmission lines replaced with microstrips and T-junctions are shown in Fig. 8. The physic parameters of the actuall layout is shown in the below TableI

TABLE I
PHYSIC PARAMETERS OF THE MICROSTIP LINES IN DESIGN(MM)

	TL1	TL2	TL3	TL4	TL5	TL6	TL7
Length	16.6	11.5	8	12	10	9.6	8.4
Width	3.4	3.4	3.4	3.4	3.4	3.4	3.4

	TL8	TL9	TL10	TL11	TL12	TL13	TL14
Length	16.6	11.5	8	12	10	9.6	8.4
Width	3.4	3.4	3.4	3.4	3.4	3.4	3.4

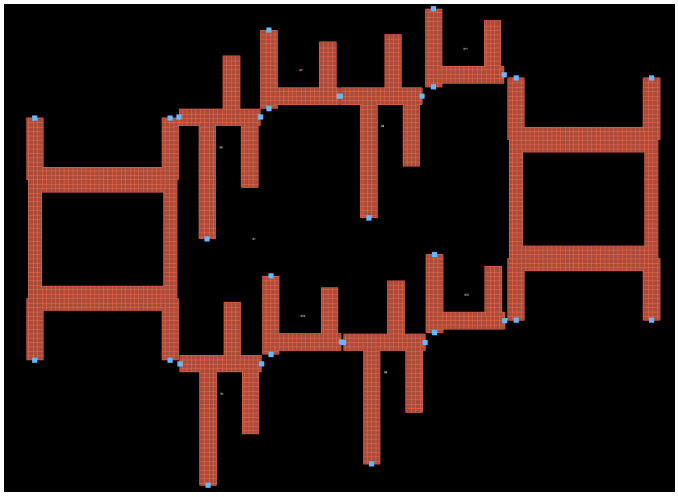

Fig. 8. Overall structure for layoutview

After the EM simulation we generated the symbol and put it back to the circuit for the post-layout simulation. The whole amplifier circuit with embedded layout is showed in Fig. x. The lumped components and bias voltage are shown in Table II.

TABLE II
PHYSIC PARAMETERS OF THE LUMPED COMPONENTS/BIAS IN DESIGN

C1	C2	C3	R1	Vdc	Vbias
2.5pF	2pF	10pF	10Ohm	28V	-3.1V

V. OVERALL SIMULATION RESULTS

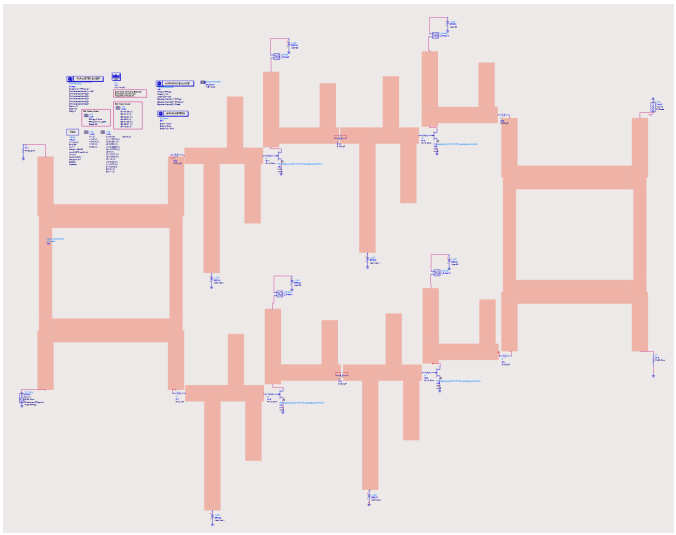

Fig. 9. Integration Simulation

In this project, our balanced 2-stage class-B power amplifier achieves a 28.3-dB power gain, 55% PAE, 43.4 dBm Psat and 600 MHz power gain bandwidth and unconditional stability with 50-ohm input and output resistance. With additional tuning, second and third harmonic rejection and the overall efficiency should be able to be further improved. We did not do it due to the time limitation. The integration simulation schematic in ADS is shown in Figure. 9. The detailed simulation results can be seen in Table II and Figure.10, also. Power bandwidth is performed using ADS HB simulation can given below in Figure. 11 which shows a power bandwidth of 600MHz:

TABLE III
SIMULATED RESULTS OF THE PROPOSED CLASS-B POWER AMPLIFIER

Simulated Results	
PAE	55%
Gain	28.3dB
Stability	Unconditional stable
Output Power	43.4dBm
P1dB	14dBm
3dB-Bandwidth	600MHz
S11	-20dB
S22	-20dB

VI. QUESTIONS & ANSWERS

A. Does the project show your understanding of the balanced power amplifier?

The project is a great opportunity to enhance our understanding of balanced power amplifier design, impedance matching and circuit optimization skills.

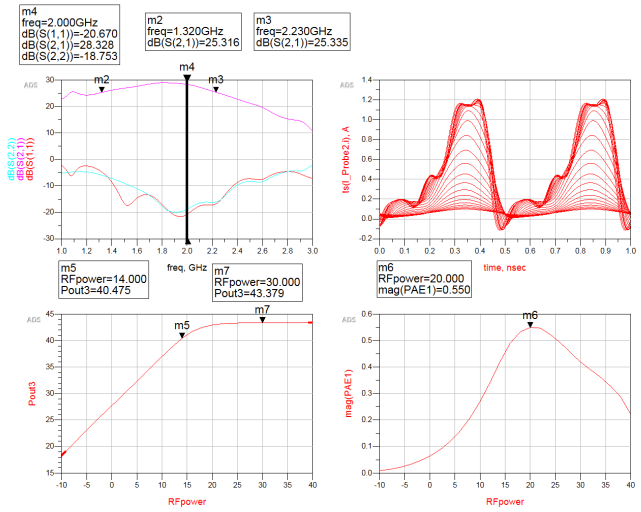

Fig. 10. Simulation results plot

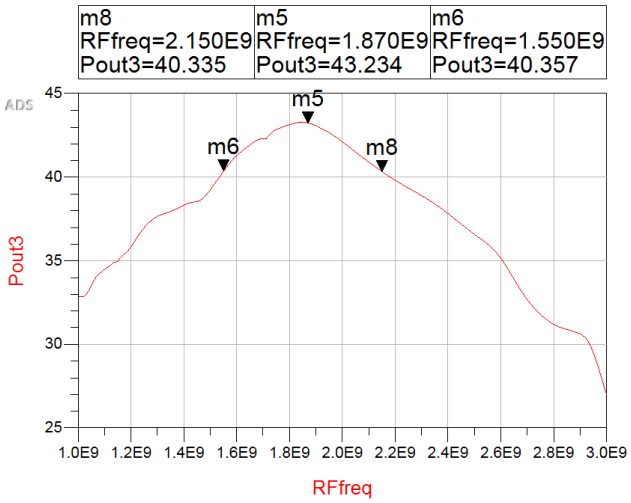

Fig. 11. Power Bandwidth

B. Why do you think your design is a class B amplifier?

The design is a class B amplifier because: 1. the transistor is biased right at the threshold voltage; 2. the current waveform shows a half-wave rectification; 3. the Keysight load-line template shows a 180-degree conduction angle and a 50% duty cycle. This can be verified in Figure.12 by checking the waveform duty cycle of the current.

C. What is the impact of hybrid coupler to the overall PAE?

Ideally, a hybrid coupler should not make any change to PAE. But in real design the hybrid coupler will be lossy and that will eventually decrese the overall efficiency.

D. How do you design the circuits and choose the values for the stubs/components?

The design follows the sequence: 1). input/output matching 2). single-stage amplifier design 3). two-stage amplifier design 4). balance two-stage amplifier design. The stubs are chosen

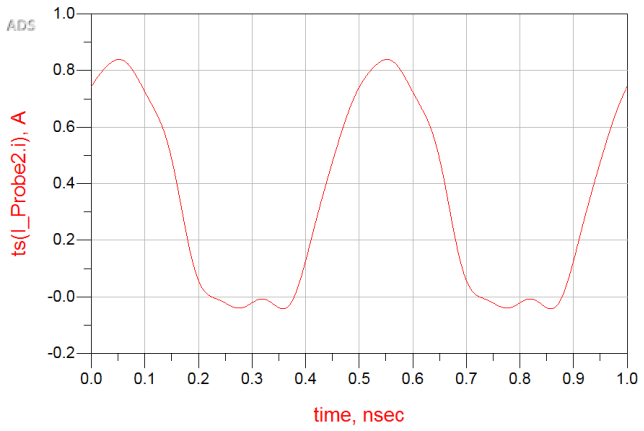

Fig. 12. Current Waveform

to render maximum possible output power and harmonics rejection.

E. How do you measure/calculate those important metrics in your design?

The power gain and -3-dB output bandwidth can be obtained by S21; PAE is calculated using the equation: (Pout-Pin)/PDC, where Pout and Pin are obtained by HB analysis and PDC is calculated using the product of DC bias voltage and current;

F. How do you optimize/tune your design and why do you want to do these optimizations/tunings?

Optimizations are mainly based on these three metrics and we also tuned circuit parameters to improve harmonic rejection and current waveform.

G. Show different designs and compare their performance?

We tried to do the interstage matching by coupled-line coupler and the post-layout simulation shows a 12% degradation in PAE and 520-MHz in bandwidth compared to our original design. Therefore we decided not to use it.

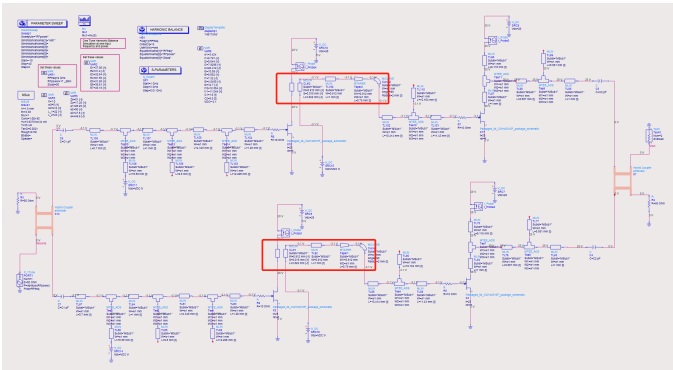

Fig. 13. Couple line matching

VII. Appendix

A. Performance (20 pts)

Does your design achieve relatively good performance? Our balanced power amplifier achieved relatively good performance in terms of gain, PAE and bandwidth. One thing that can be improved is that the second and third harmonic termination are not perfect, and the harmonic rejections are above -40dB. This can be mitigated by careful tuning of matching networks.

B. Participation (15 pts)

Both students in the group fully participated in the project with close collaboration.

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